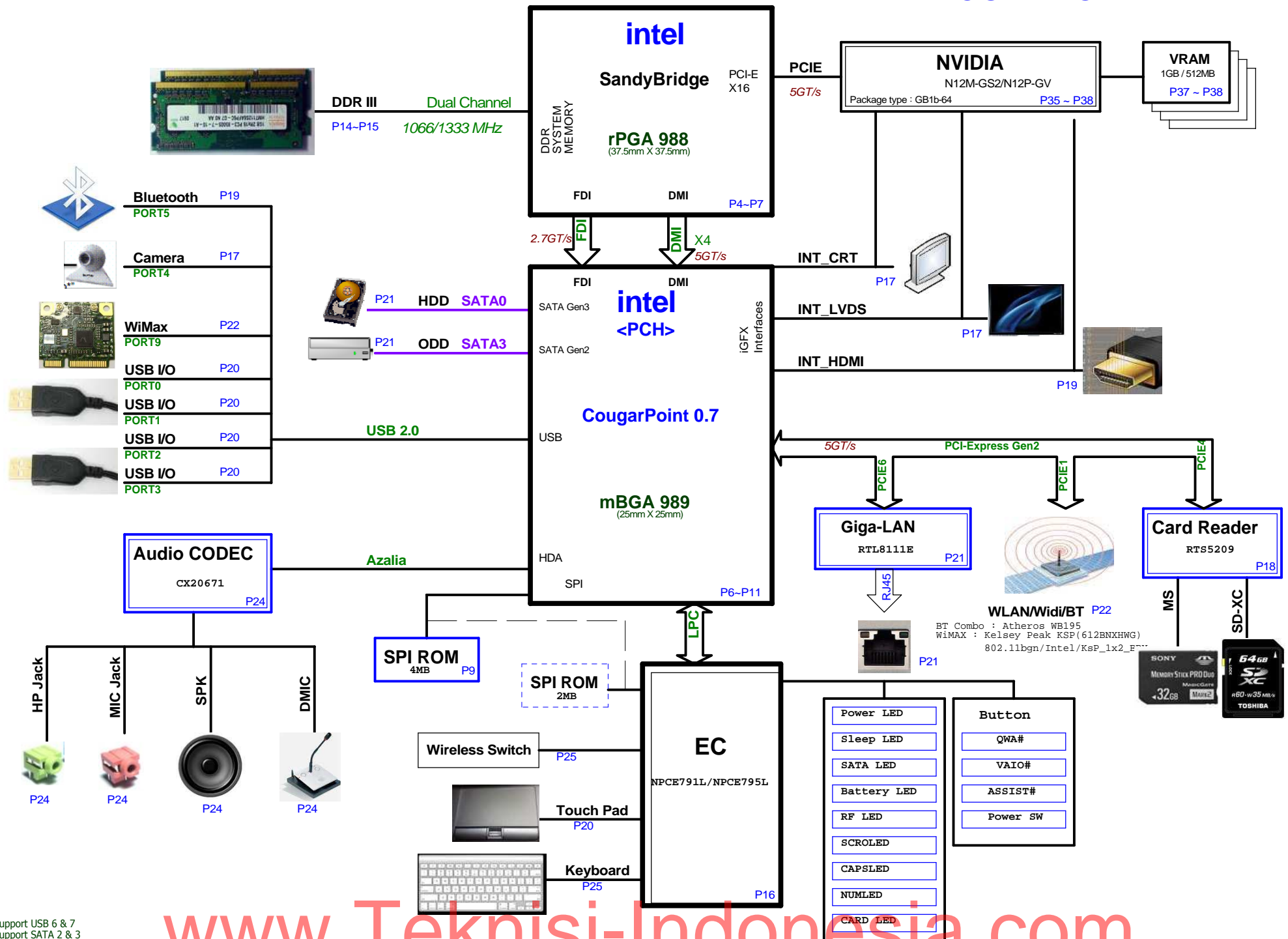


\* : No mount  
 E@ : For DIS GFX only  
 I@ : For INT GFX only

Page	Title of schematic page	Rev.	Date
01	Page List	1A	
02	Block Diagram	1A	
03	Change List	1A	
04	SNB 1/4(HOST&PCIE)	1A	
05	SNB 2/4(DDR3 I/F)	1A	
06	SNB 3/4(POWER)	1A	
07	SNB 4/4(GND/Strap)	1A	
08	PCH 1/6(DMI/FDI/VIDEO)	1A	
09	PCH 2/6(SATA/RTC/HDA/LPC)	1A	
10	PCH 3/6(PCIE/USB/CLK/NV)	1A	
11	PCH 4/6(GPIO/CPU/STRAP)	1A	
12	PCH 5/6(POWER)	1A	
13	PCH 6/6 (GND)	1A	
14	DDR3 DIMM-0-STD	1A	
15	DDR3 DIMM-1-STD	1A	
16	WPCE791L & FLASH	1A	
17	CRT/LVDS/CAMERA	1A	
18	CARD READER(RTS5209)	1A	
19	HDMI Conn/BT/THERMAL	1A	
20	USB/TP/FAN	1A	
21	LAN (RTL8111E)	1A	
22	WLAN/HOLE	1A	
23	HDD/ODD/EMI	1A	
24	Audio CX20671	1A	
25	LED/RF/KB/PS	1A	
26	POWER +VCC_CORE (ISL95831)	1A	
27	POWER 3VPCU&5VPCU(PM6686)	1A	
28	POWER 1.5VSUS/VTT_MEM	1A	
29	POWER +1.05V(UP6128A)-15A	1A	
30	POWER +0.85V(APE8858)-6A	1A	
31	POWER VGA_CORE(OZ8111)--15A	1A	
32	POWER VCC1.8/Thermal	1A	
33	POWER(ADAPTER IN / CONN)	1A	
34	POWER CHARGER (ISL88731C)	1A	
35	NVIDIA GS2-64 PCIE&PW 1/4	1A	
36	NVIDIA GS2-64 TMDS&DAC 2/4	1A	
37	NVIDIA GS2-64 VRAM 3/4	1A	
38	NVIDIA GS2-64 VRAM 4/4	1A	
39	IO PORT LIST	1A	

## HK1 BLOCK DIAGRAM



Change List from PVT to MP

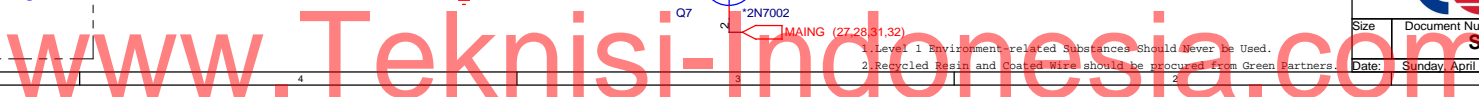
HK1\_MB\_SCH\_PVT\_001

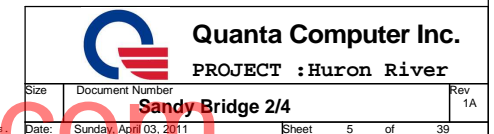
P19-- R345 change to 48.7K.  
Reason : Change thermal sensor temperature to 55 degree.  
Possible Risk: No.

P19-- R208 change to 27.4K for UMA.  
Reason : Change thermal sensor temperature to 82 degree.  
Possible Risk: No.

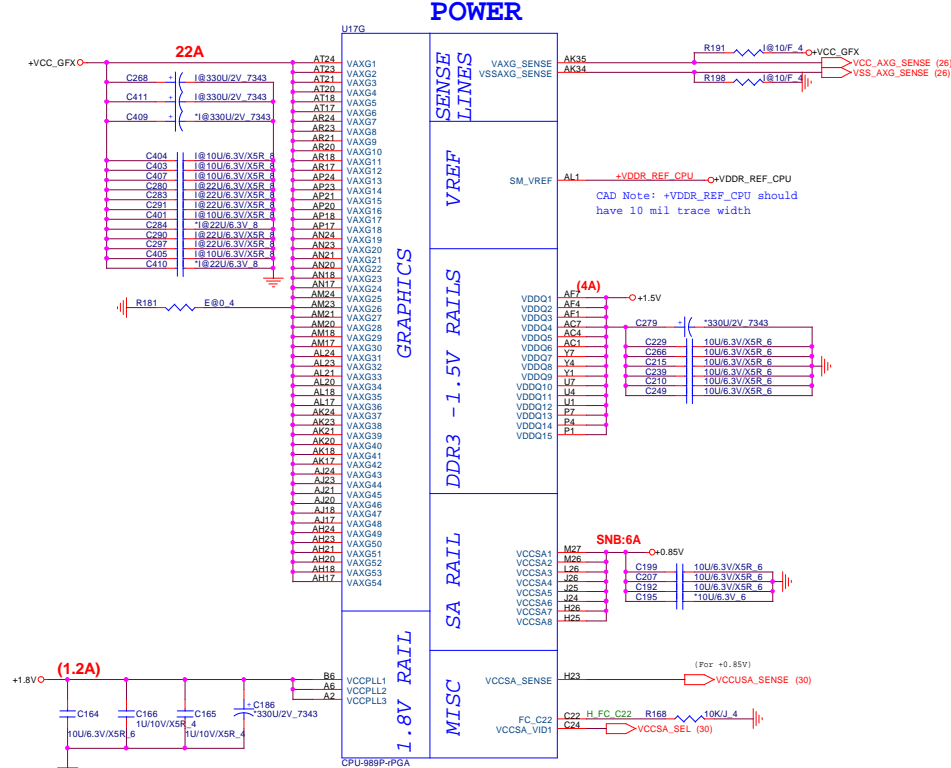
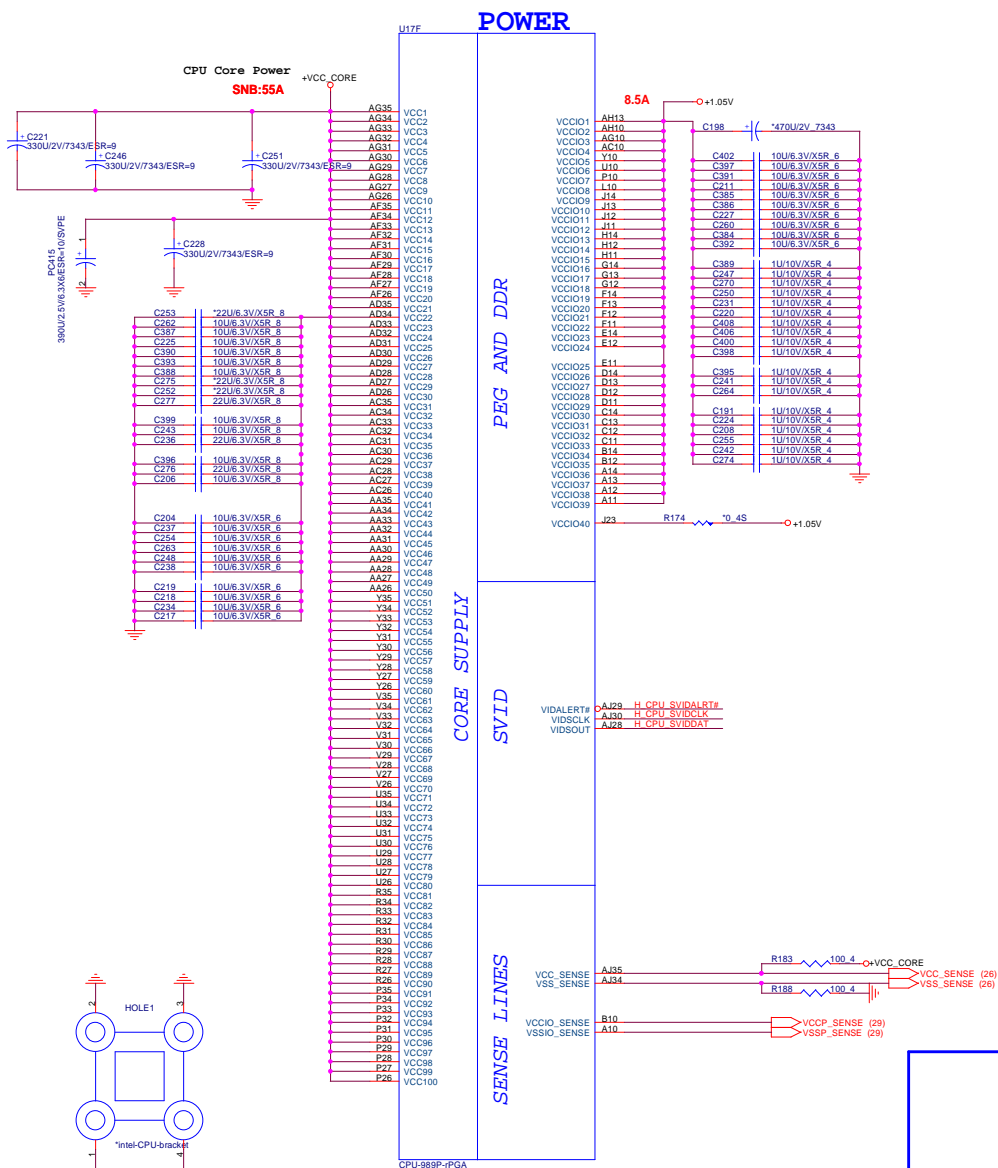
HK1\_MB\_SCH\_PVT\_002

P16-- KR27 change value from 10K to 4.7K.  
P33-- PD7 change value from uClamp3301D to CDSOD323-T03C.  
Reason : for Battery ESD protect.  
Possible Risk: No.





Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT needs to be between CLK and DATA

**SVID CLK**

0.05V

- Place PU resistor close to

## SVID DATA

0.05V

- Place PU resistor close to CPU

**SVID ALERT**



Quanta Computer Inc.

PROJECT :Huron River

ent Number  
**Sandy Bridge 3/4**

Size	Document Number	Rev
	<b>Sandy Bridge 3/4</b>	1A

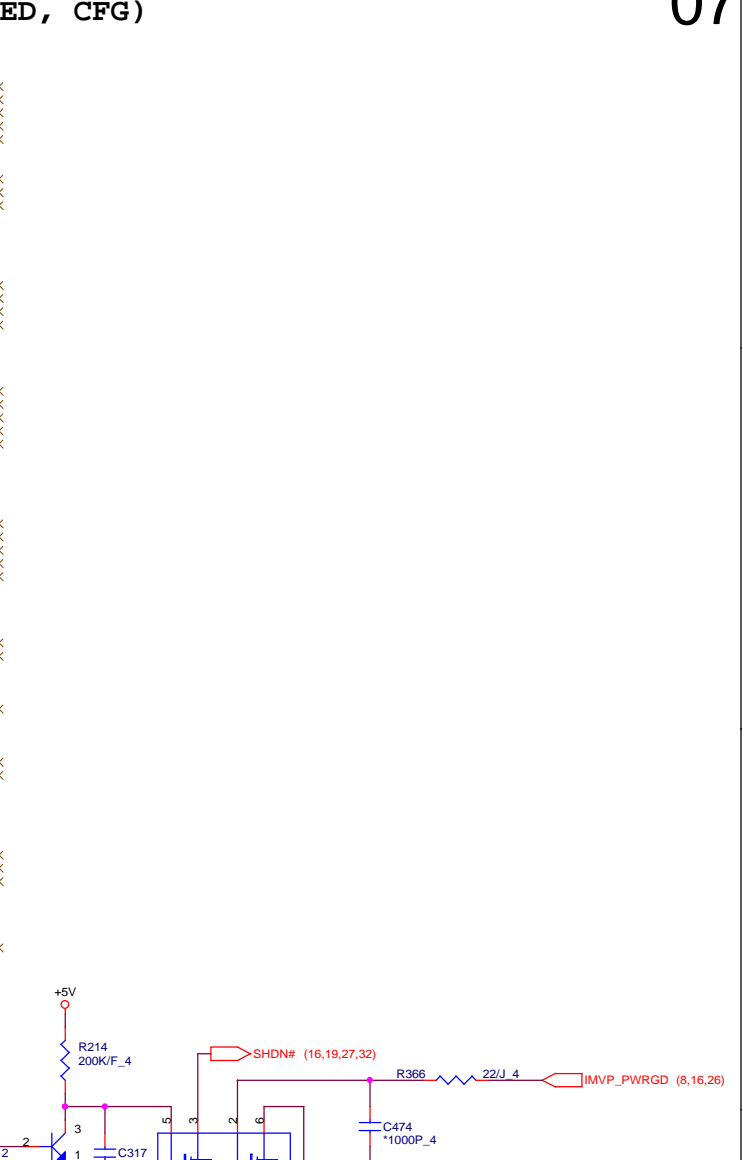
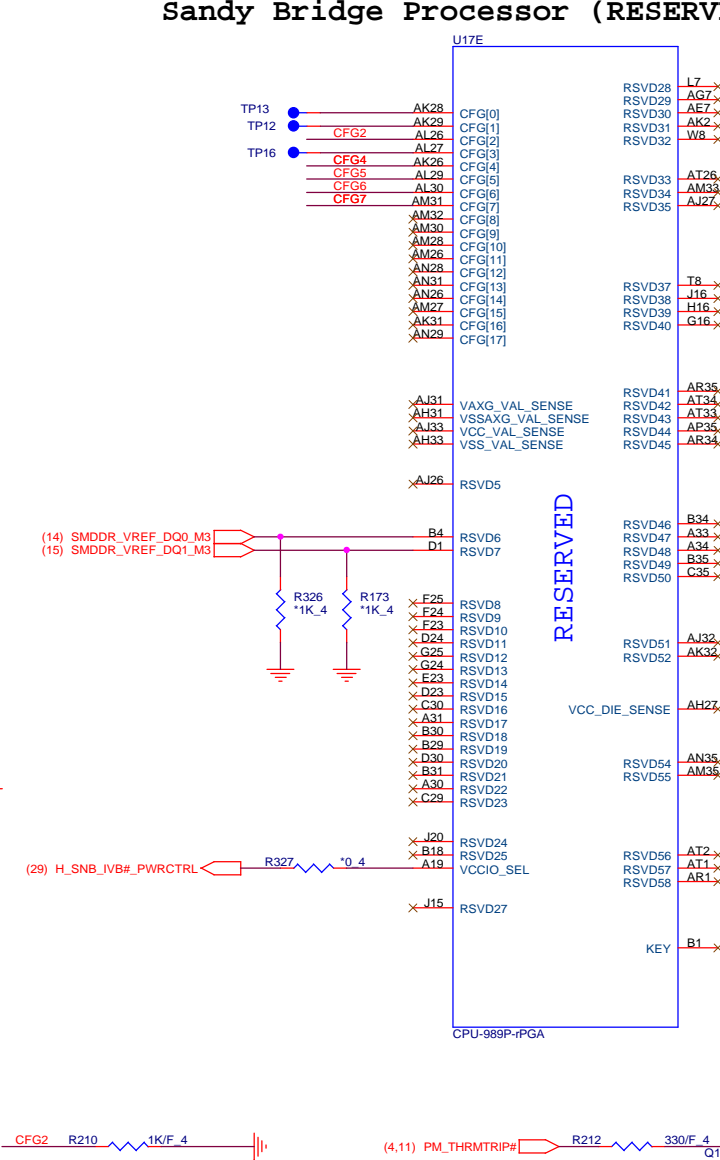
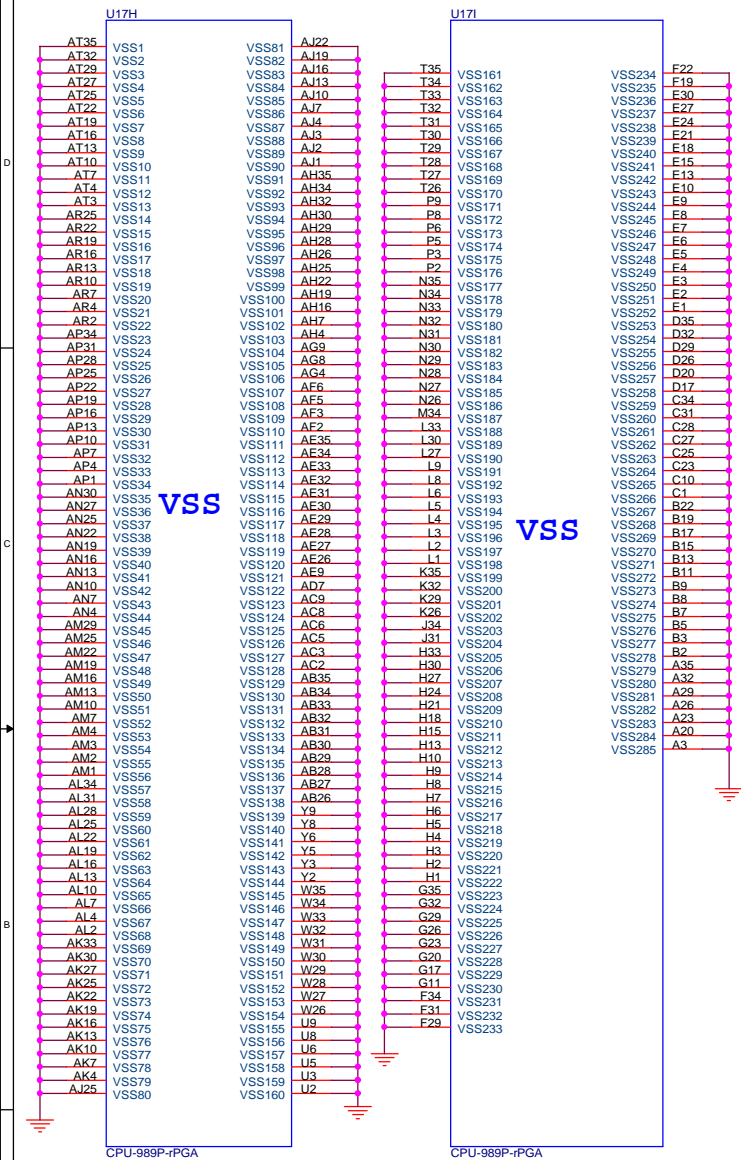
Date: Monday, February 21, 2011 Sheet 6 of 39

[illegible]



# Sandy Bridge Processor (GND)

# Sandy Bridge Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG5 R194 1K/F 4  
CFG6 R193 1K/F 4

CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface  
10: PEG x8 x8 bifurcation enabled/disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

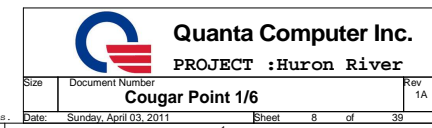
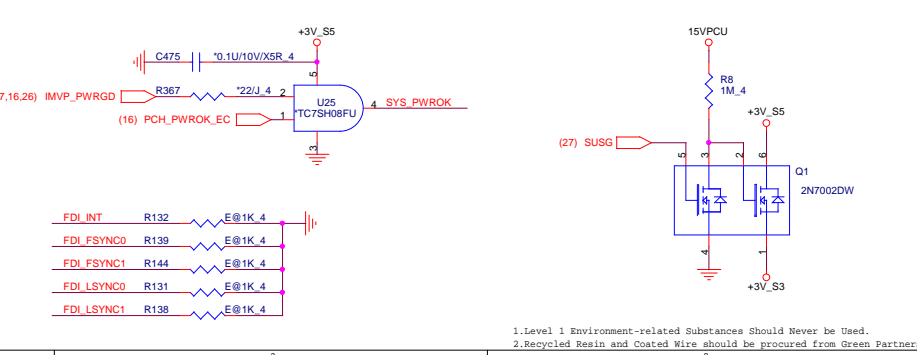
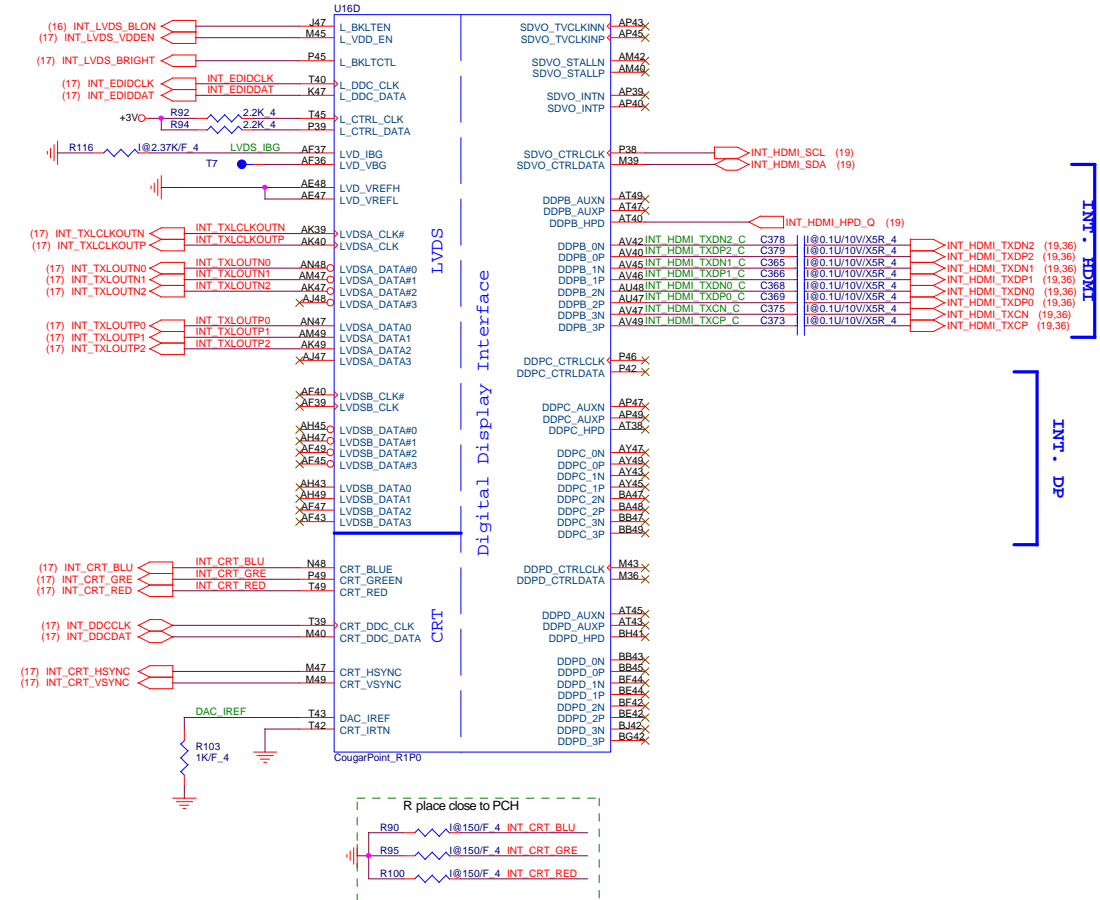
Quanta Computer Inc.

PROJECT :Huron River

Sandy Bridge 4/4

Size Document Number

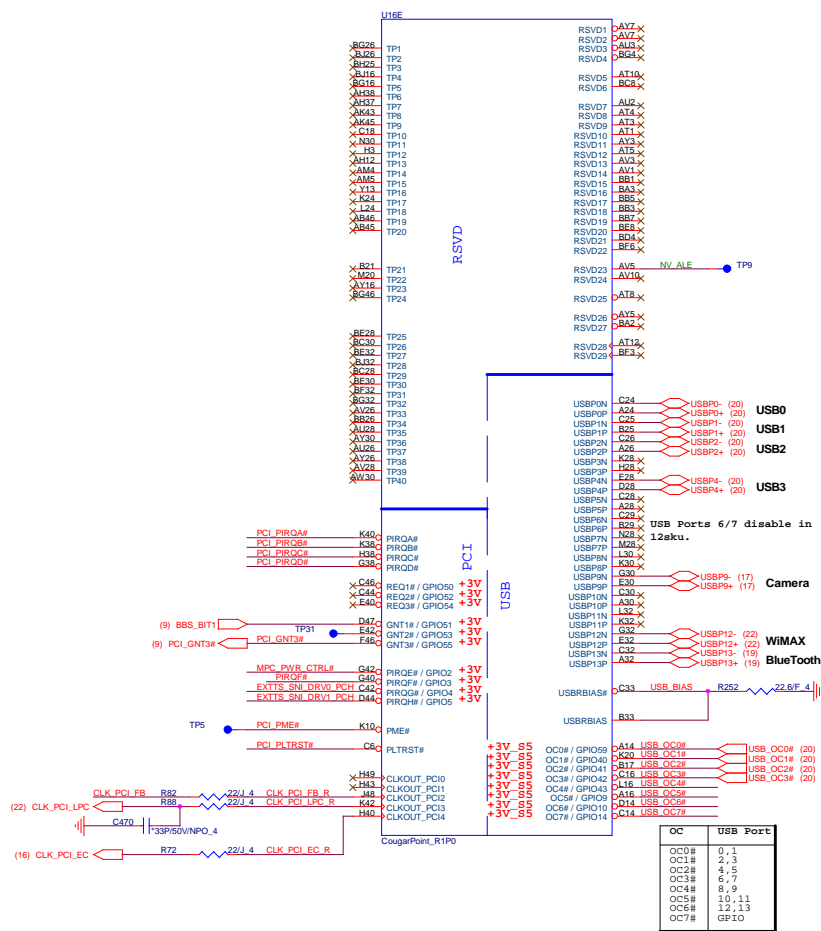
Date: Monday, February 21, 2011 Sheet 7 of 39



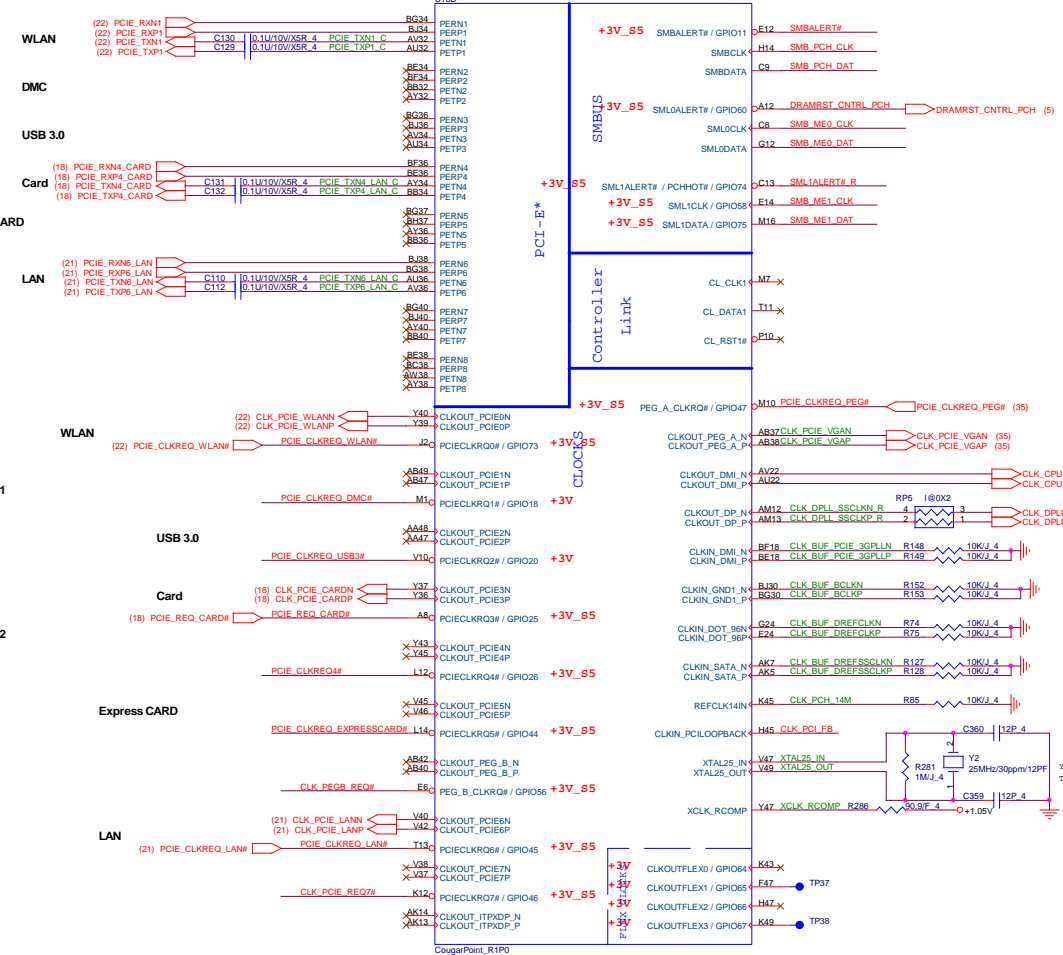




Cougar Point-M (PCI,USB,NVRAM)



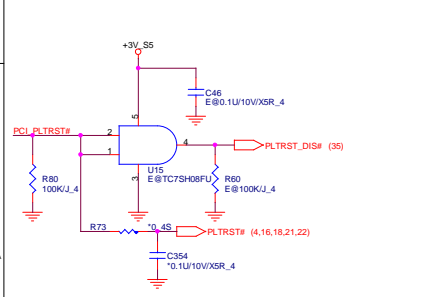
Cougar Point-M (PCI-E,SMBUS,CLK)



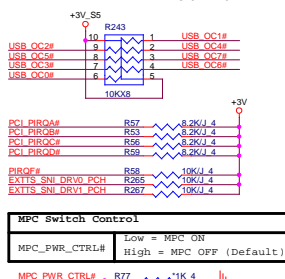
For LAN

For EC

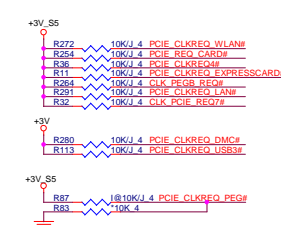
PLTRST#(CLG)



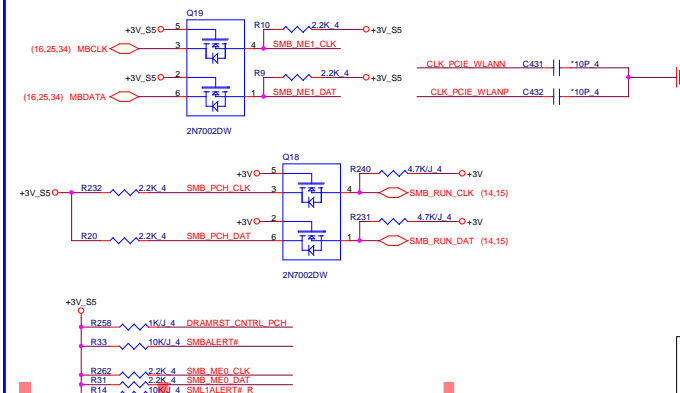
PCI/USBOC# Pull-up(CLG)



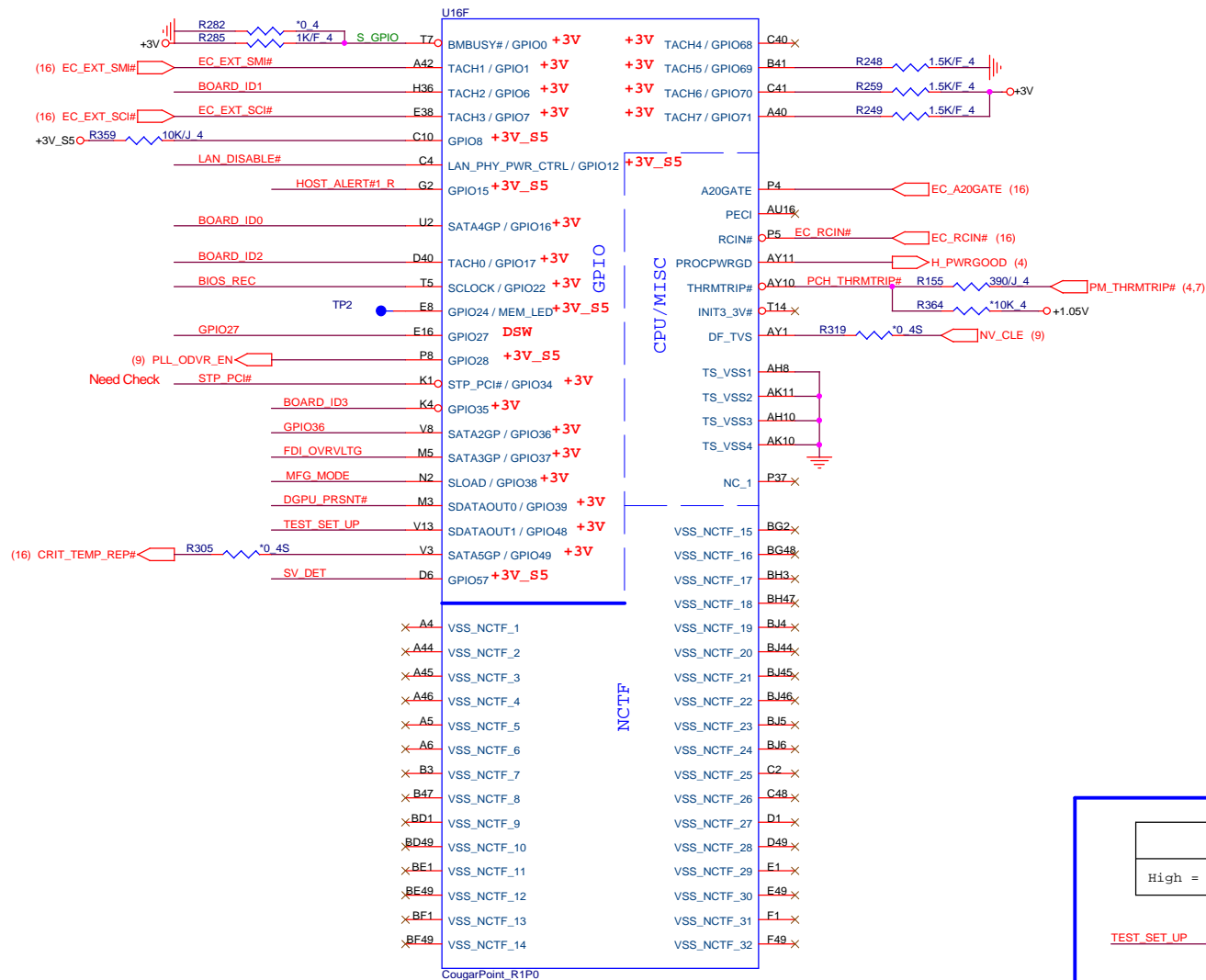
**CLK\_REQ/Strap Pin(CLG)**



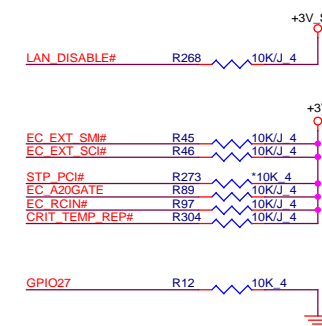
### SMBus/Pull-up(CLG)



# Cougar Point (GPIO,VSS\_NCTF,RSVD)



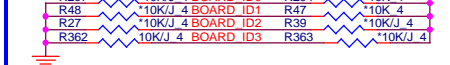
## GPIO Pull-up/Pull-down(CLG)



Board ID0 (N12M/N12P)	N12M	N12P
R294	Stuff	No Stuff
R297	No Stuff	Stuff

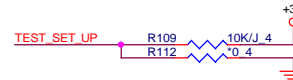
Board ID1 (VRAM Vendor)	Samaung	Hynix
R47	Stuff	No Stuff
R48	No Stuff	Stuff

Board ID2 (VRAM 1G/512M)	1G	512M
R39	Stuff	No Stuff
R27	No Stuff	Stuff



SV\_SET\_UP

High = Strong (Default)



HOST\_ALERT#1\_R

Intel ME Crypto Transport Layer Security (TLS) cipher suite

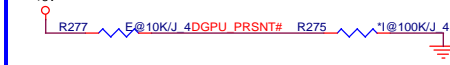
Low = Disable (Default)

High = Enable

## MFG-TEST



PCBA SKU	Discrete	UMA
R277	Stuff	No Stuff
R275	No Stuff	Stuff



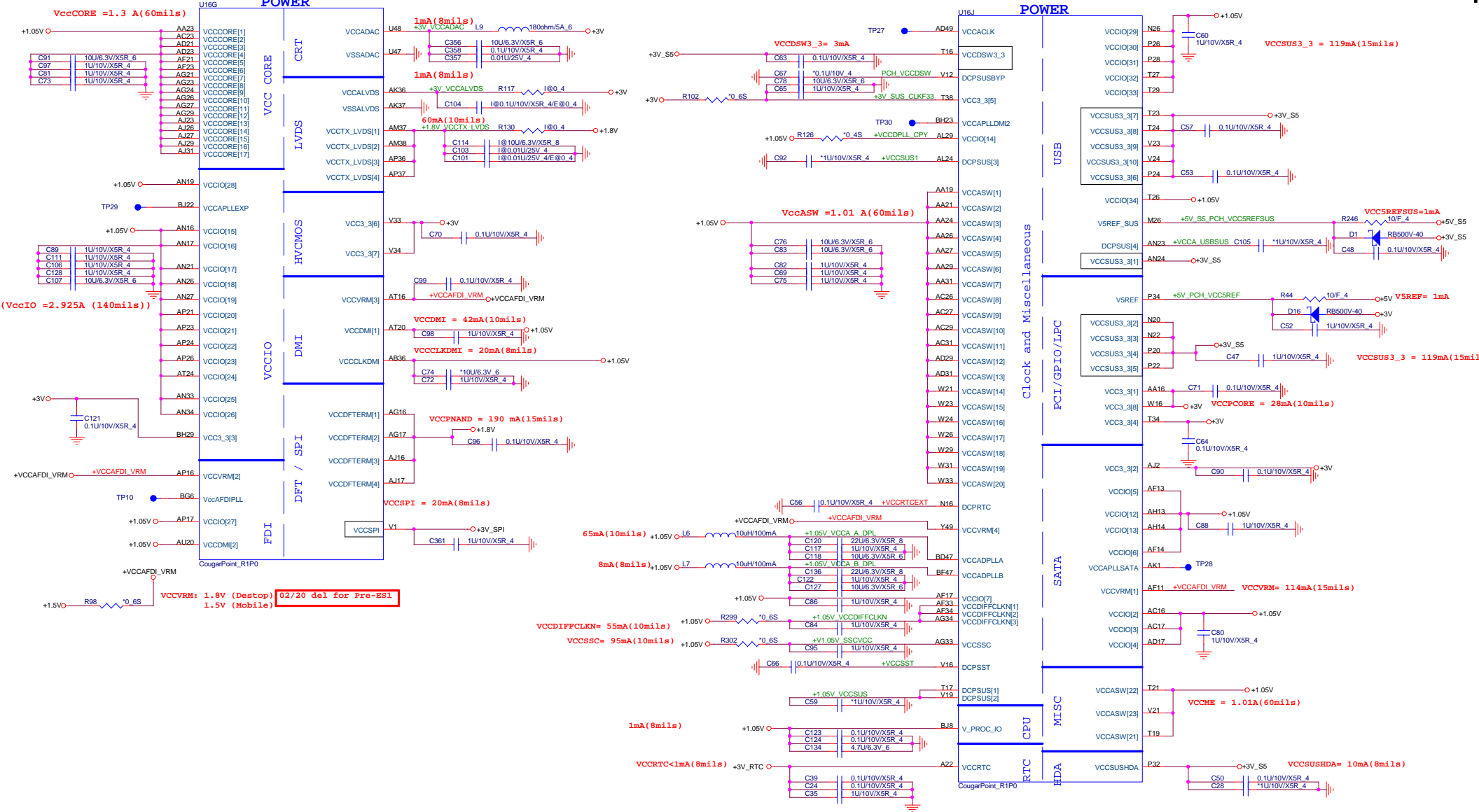
Quanta Computer Inc.


PROJECT :Huron River

Cougar Point 4/6

PCH5 (CLG) COUGAR POINT (POWER)

Cougar Point-M (POWER)

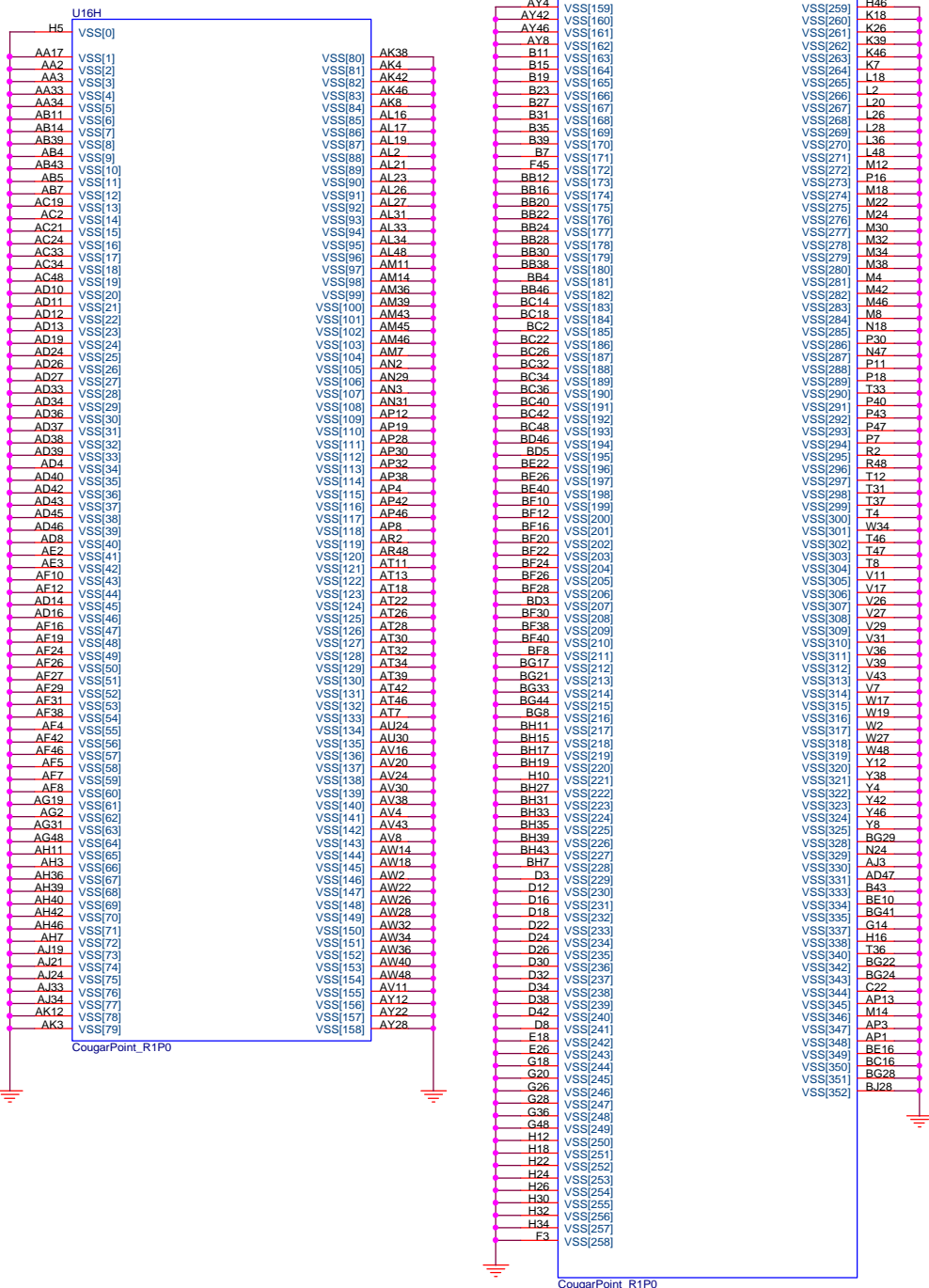




**Quanta Computer Inc.**

PROJECT :Huron River

Size	Document Number	Rev
	<b>Cougar Point 5/6</b>	1A
Date:	Tuesday, April 05, 2011	Sheet 12 of 39

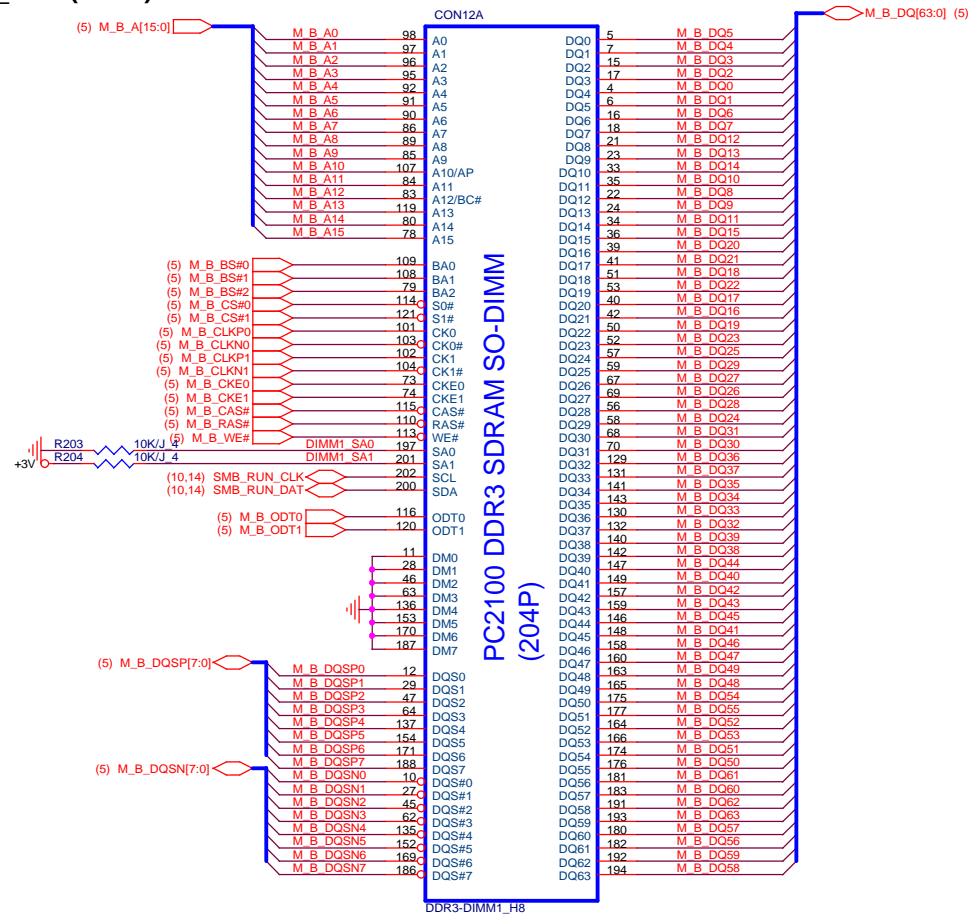




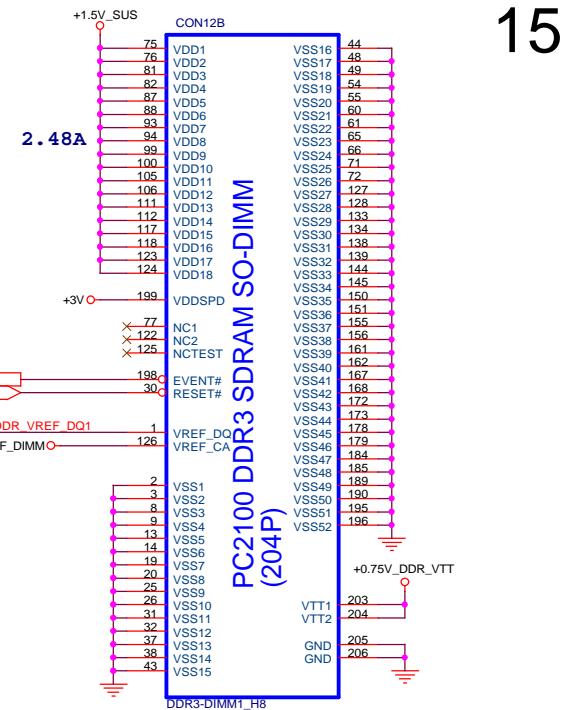




# DDR\_RVS (DDR)

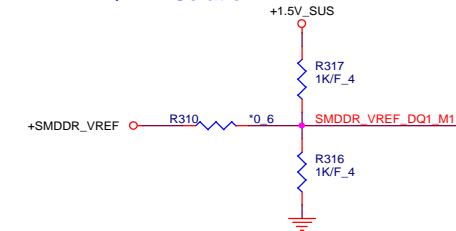


RUV Type

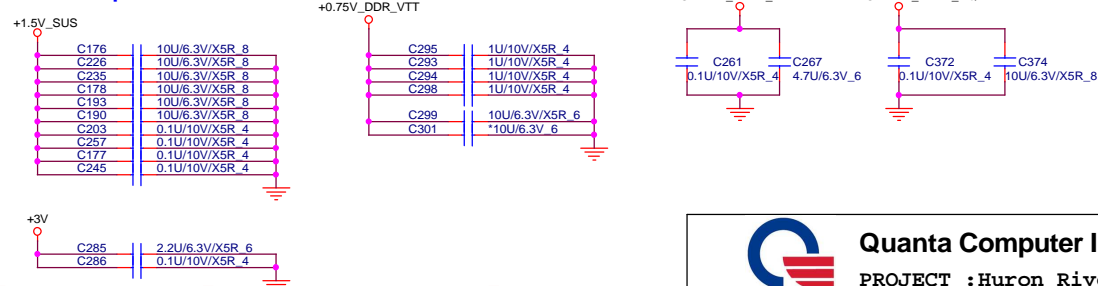


RUV Type

## VREF DQ1 M1 Solution



## Place these Caps near So-Dimm1.



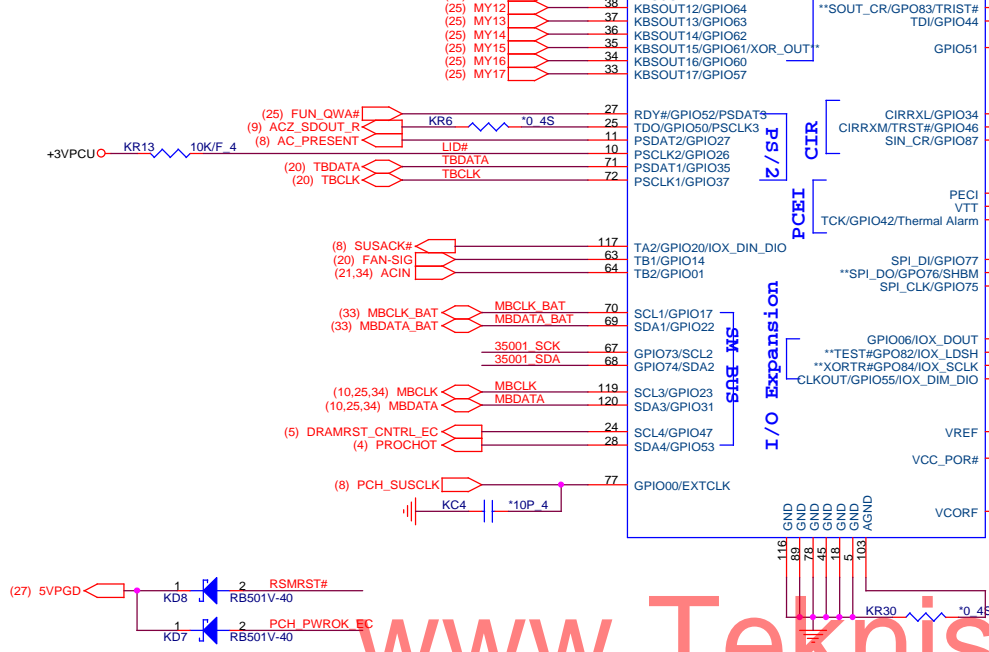
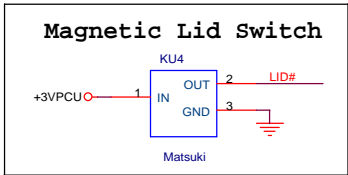
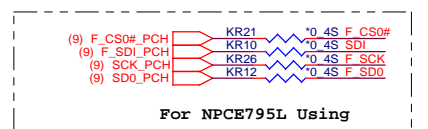
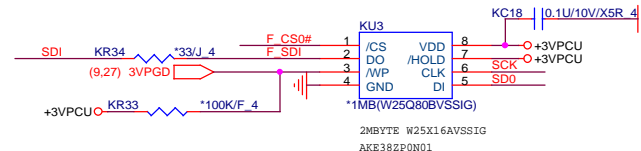
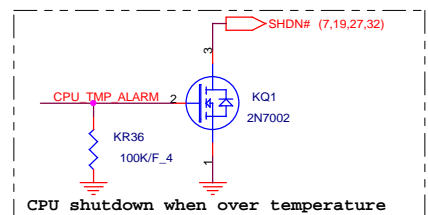
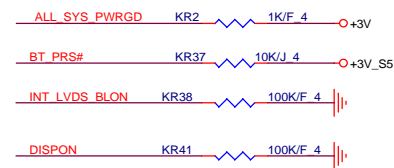
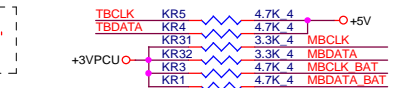
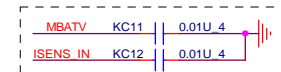
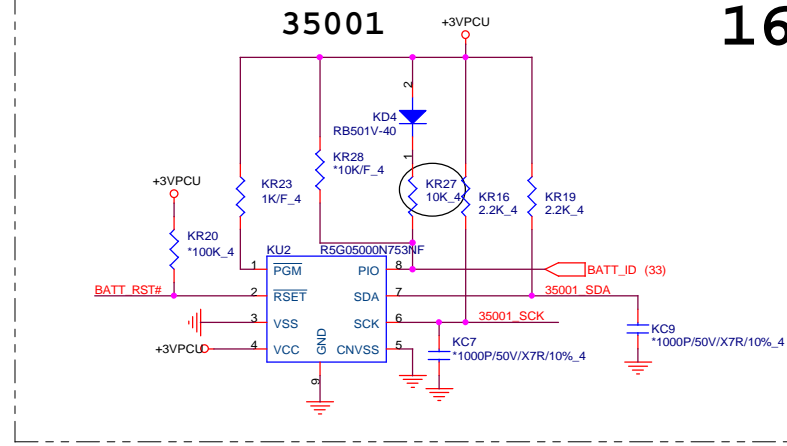
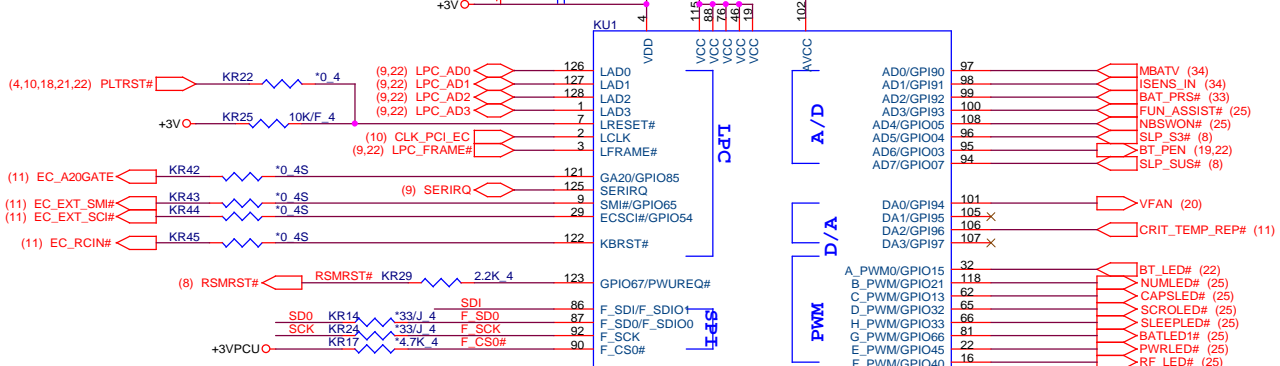
Quanta Computer Inc.

PROJECT :Huron River

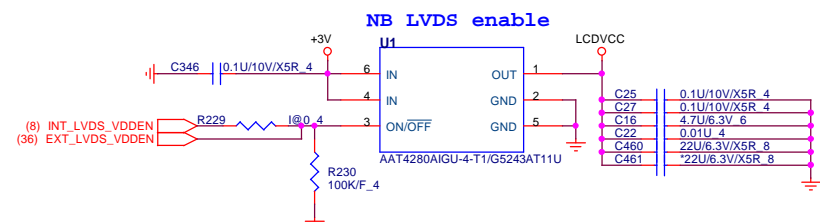
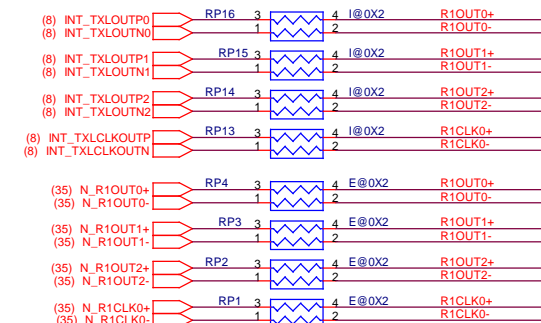
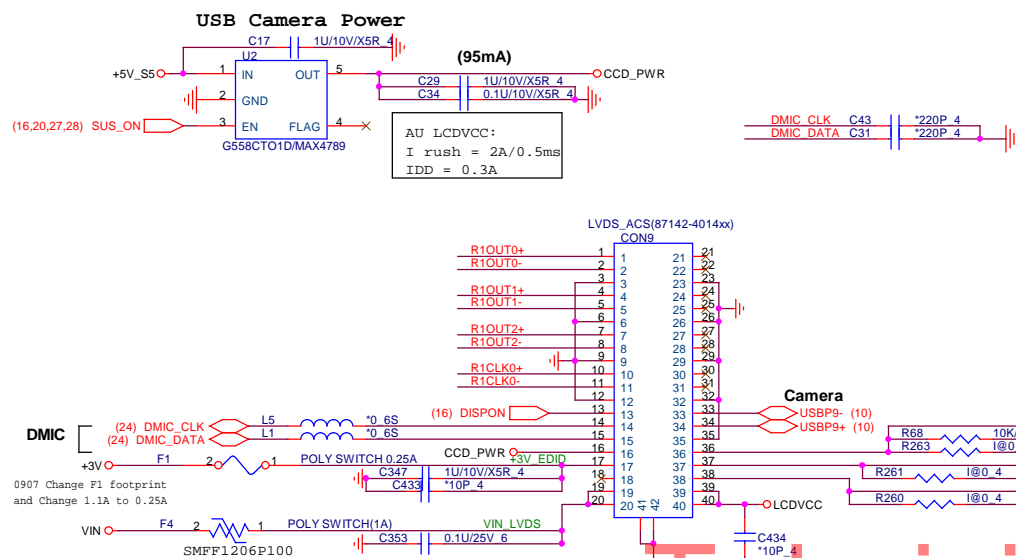
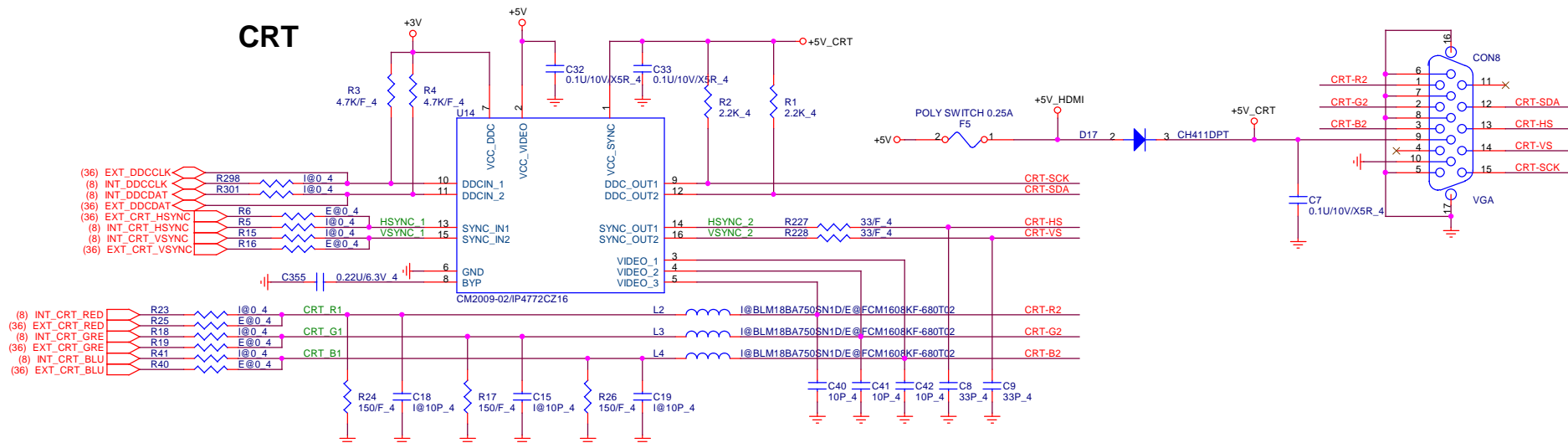
Size	Document Number	Date	Sheet	of	Rev
	DDR3 SO-DIMM-1	Tuesday, April 05, 2011	15	39	1A

Note the input leakage current to the strap pins must be less than 10uA.

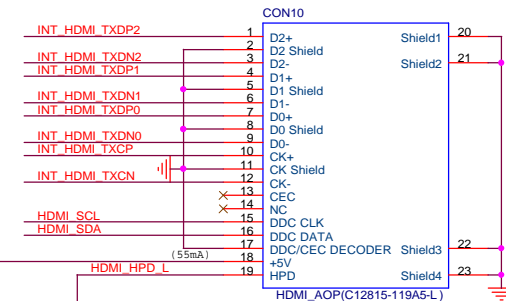
The schematic diagram illustrates the +3V\_PCPU power plane. It features a +3V\_PCPU input connected to a network of capacitors (KC17, KC5, KC14, KC8, KC3, KC10) and an inductor (KL1) with a value of 0.8S. The network is connected to a 3V\_PCPU ITE AVDD output, which is also connected to capacitors KC16 (10U6.3V/X5R\_8) and KC13 (0.1U/10V/X5R\_4).



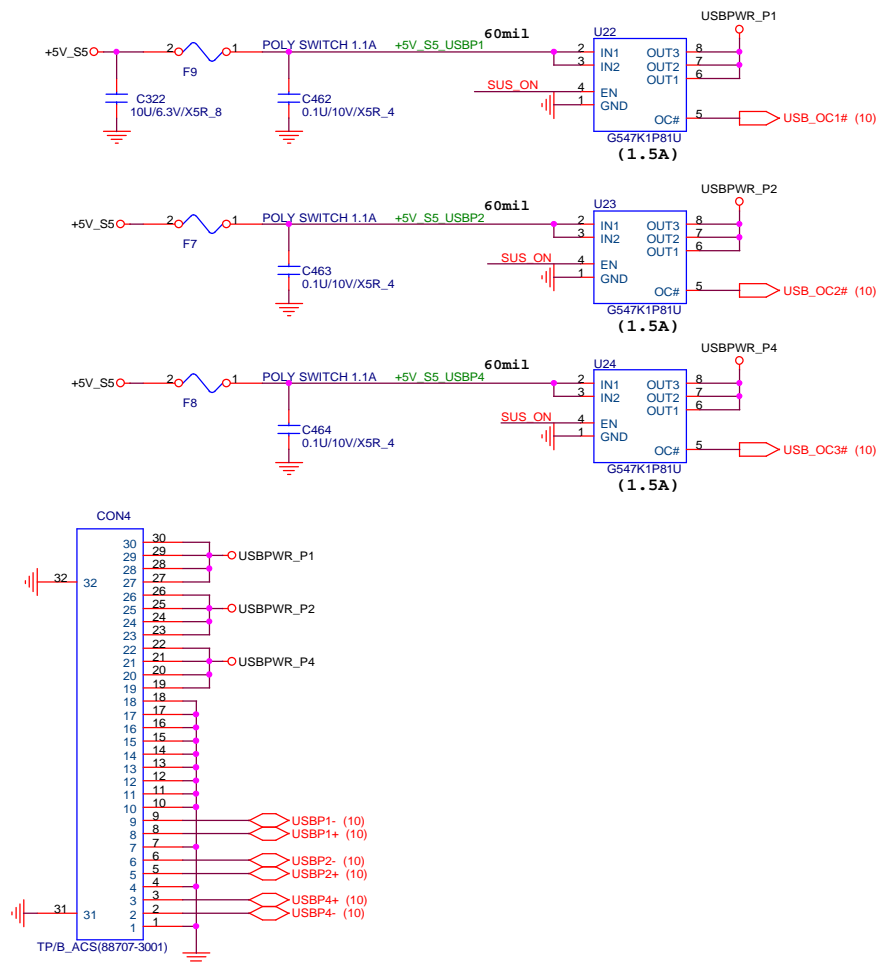
## CRT





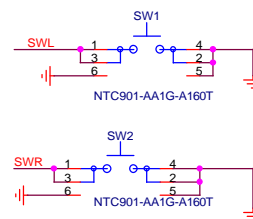
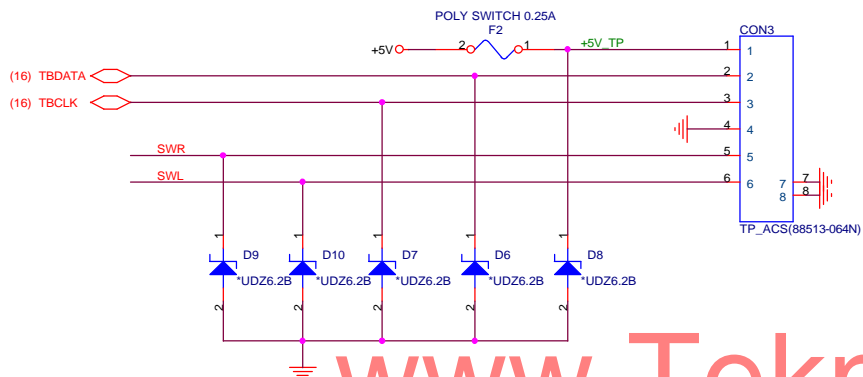


## MB to USB board



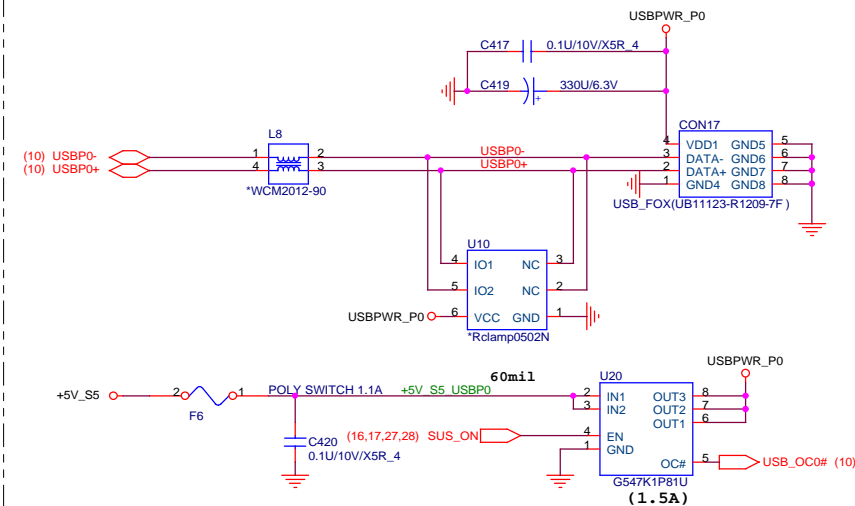
## T/P Board to T/P

9/13 change F2 P/N from 0.12A to 0.25A

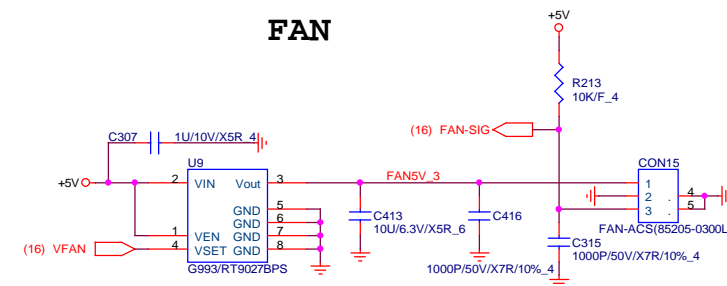


## USB PORT 0

20



## FAN



Quanta Computer Inc.

PROJECT :Huron River

USB/TP/FAN

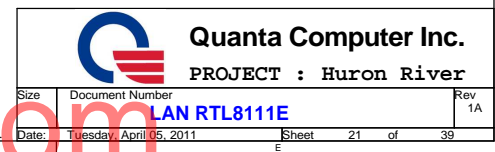
Size Document Number

Date: Monday, February 21, 2011

Sheet 20 of 39

Rev 1A

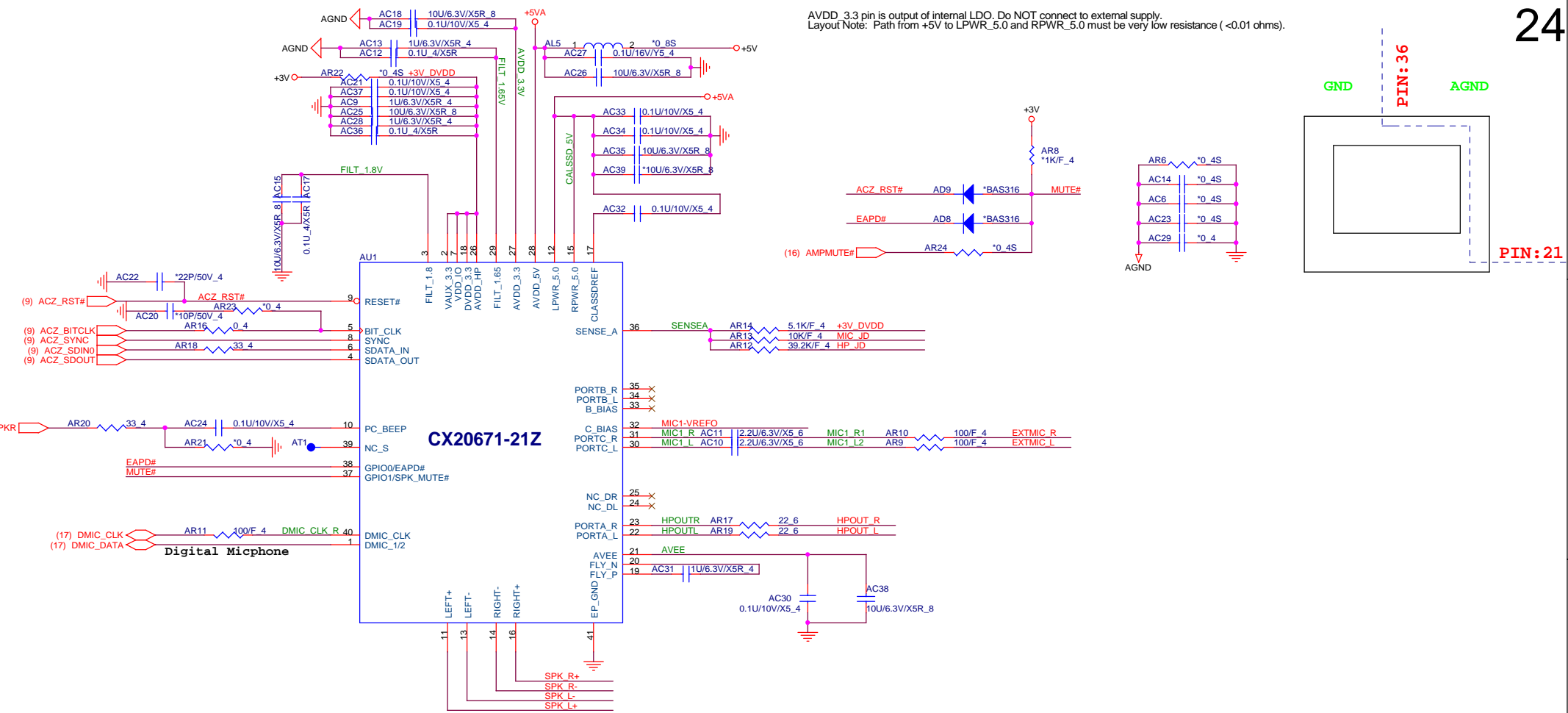




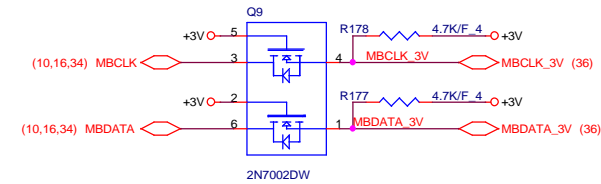




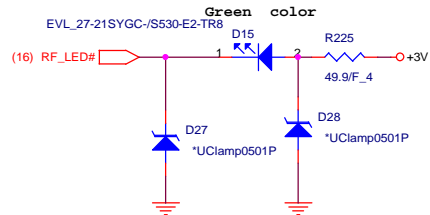
AVDD\_3.3 pin is output of internal LDO. Do NOT connect to external supply.  
Layout Note: Path from +5V to LPWR\_5.0 and RPWR\_5.0 must be very low resistance (<0.01 ohms).



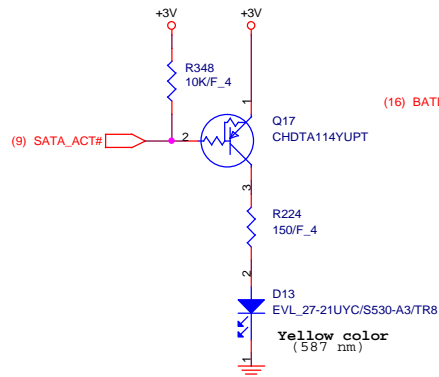
## WIRELESS/Bluetooth SWITCH



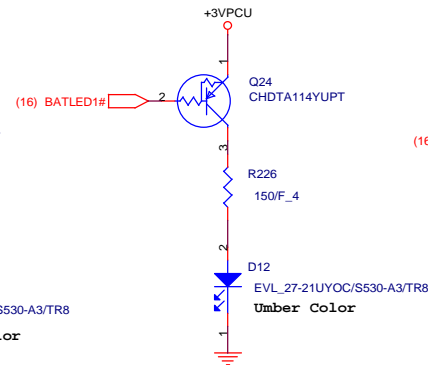
## RF LED



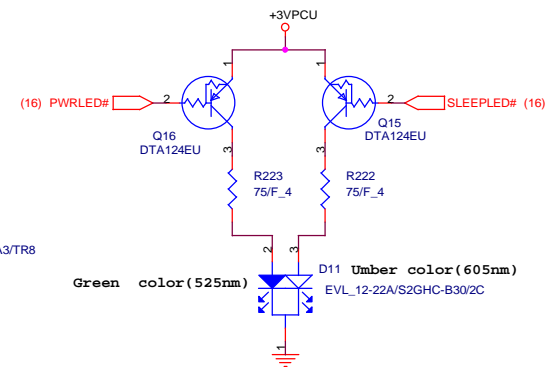
## SATA LED



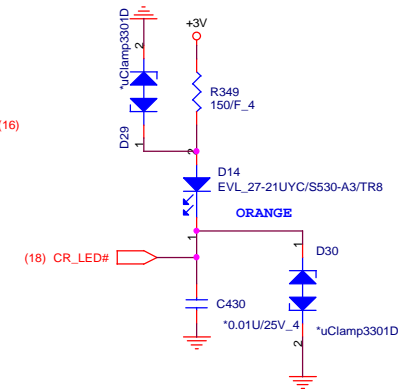
## BATTERY LED



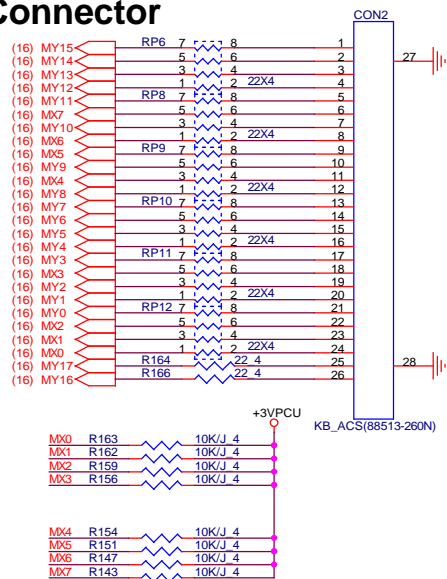
## Power/Sleep LED



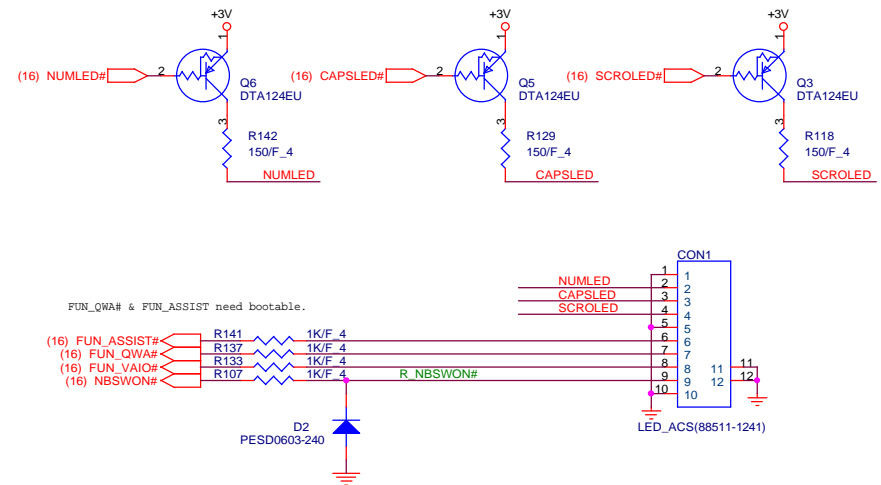
## CARD LED

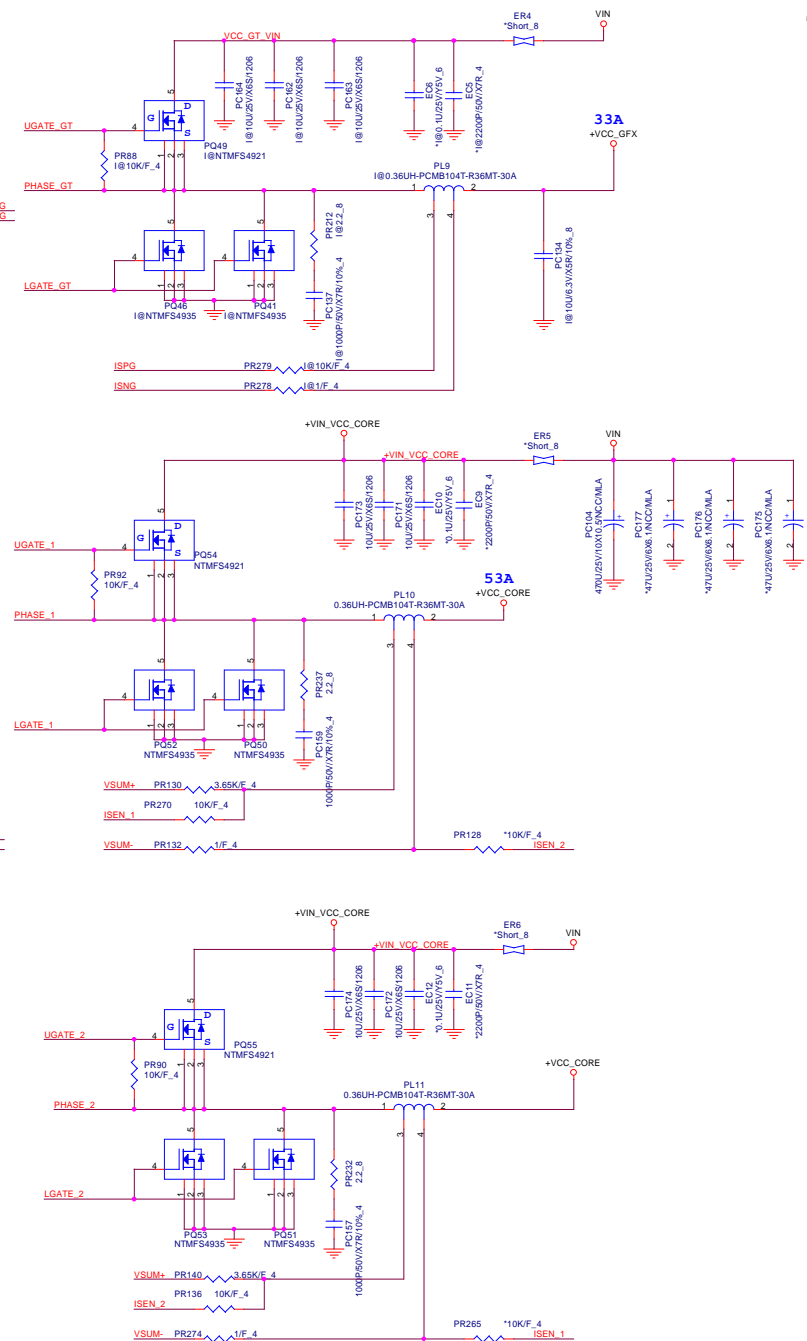


## KEY BOARD Connector

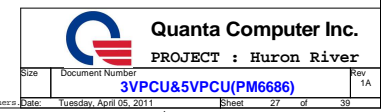


## Power SW Board Connector

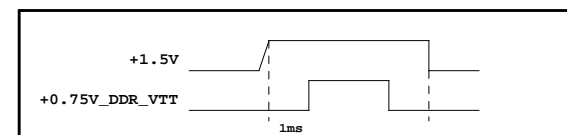
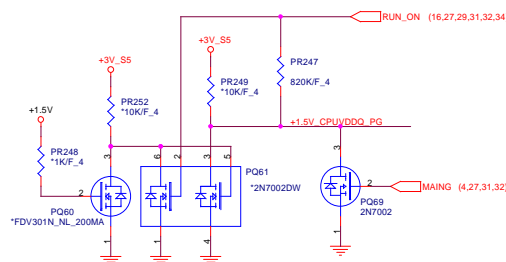
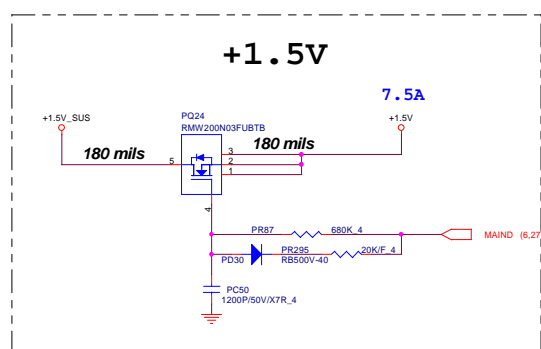
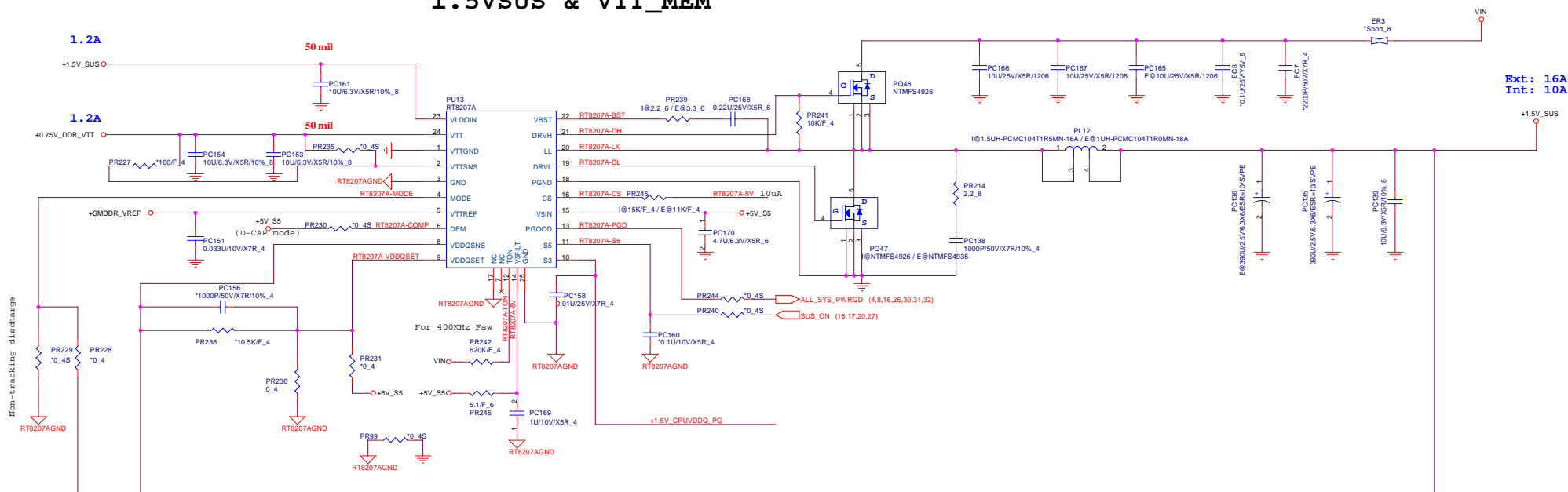








## 1.5VSUS & VTT\_MEM

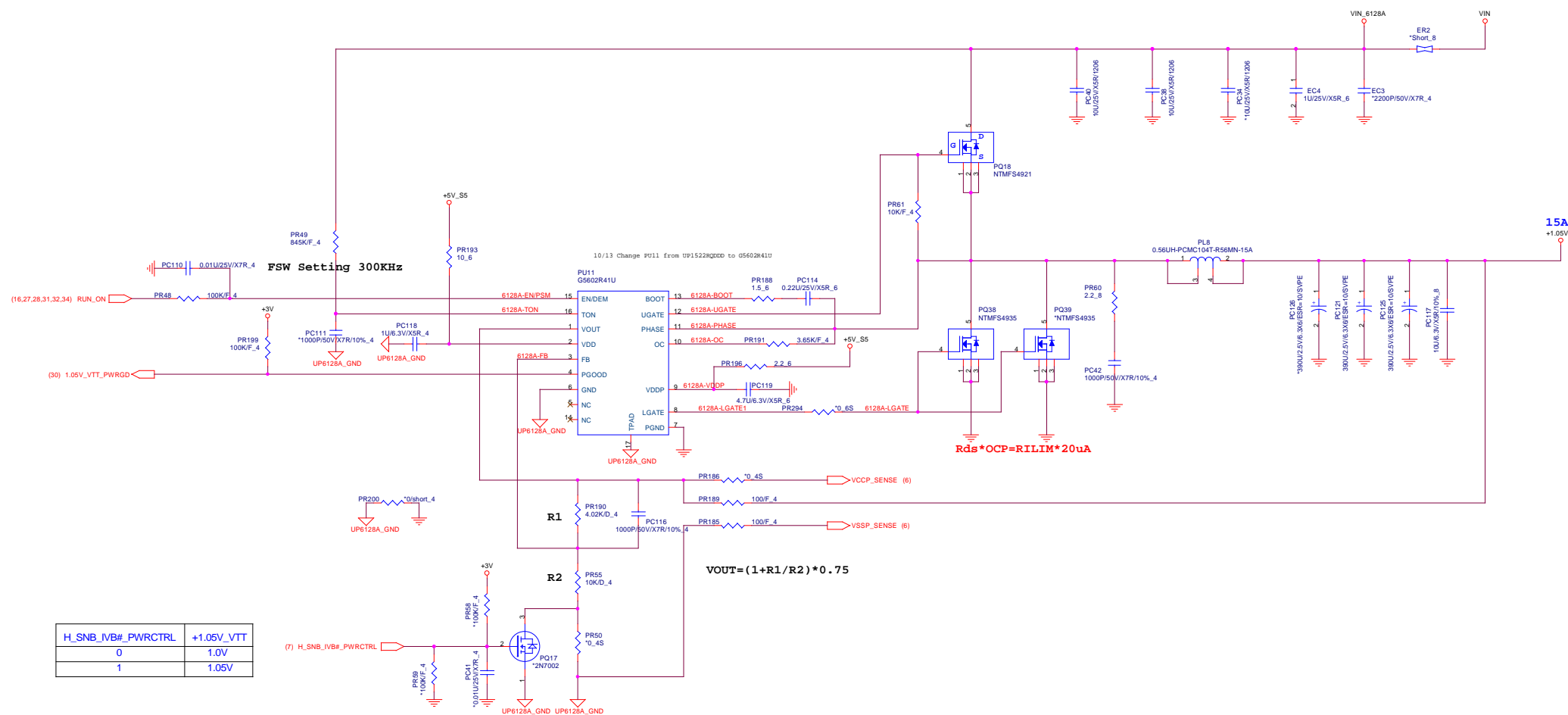


MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

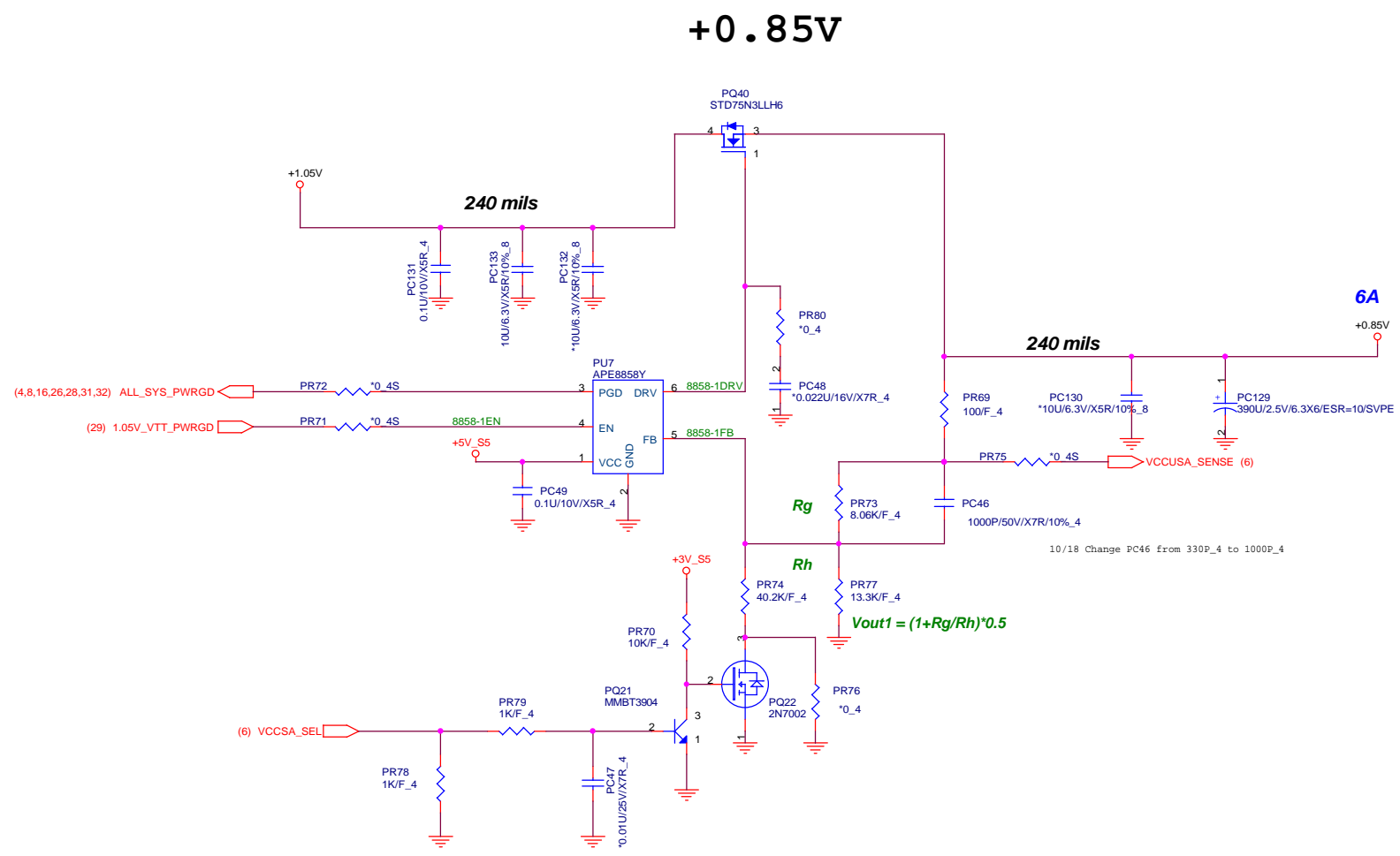
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.75V$$

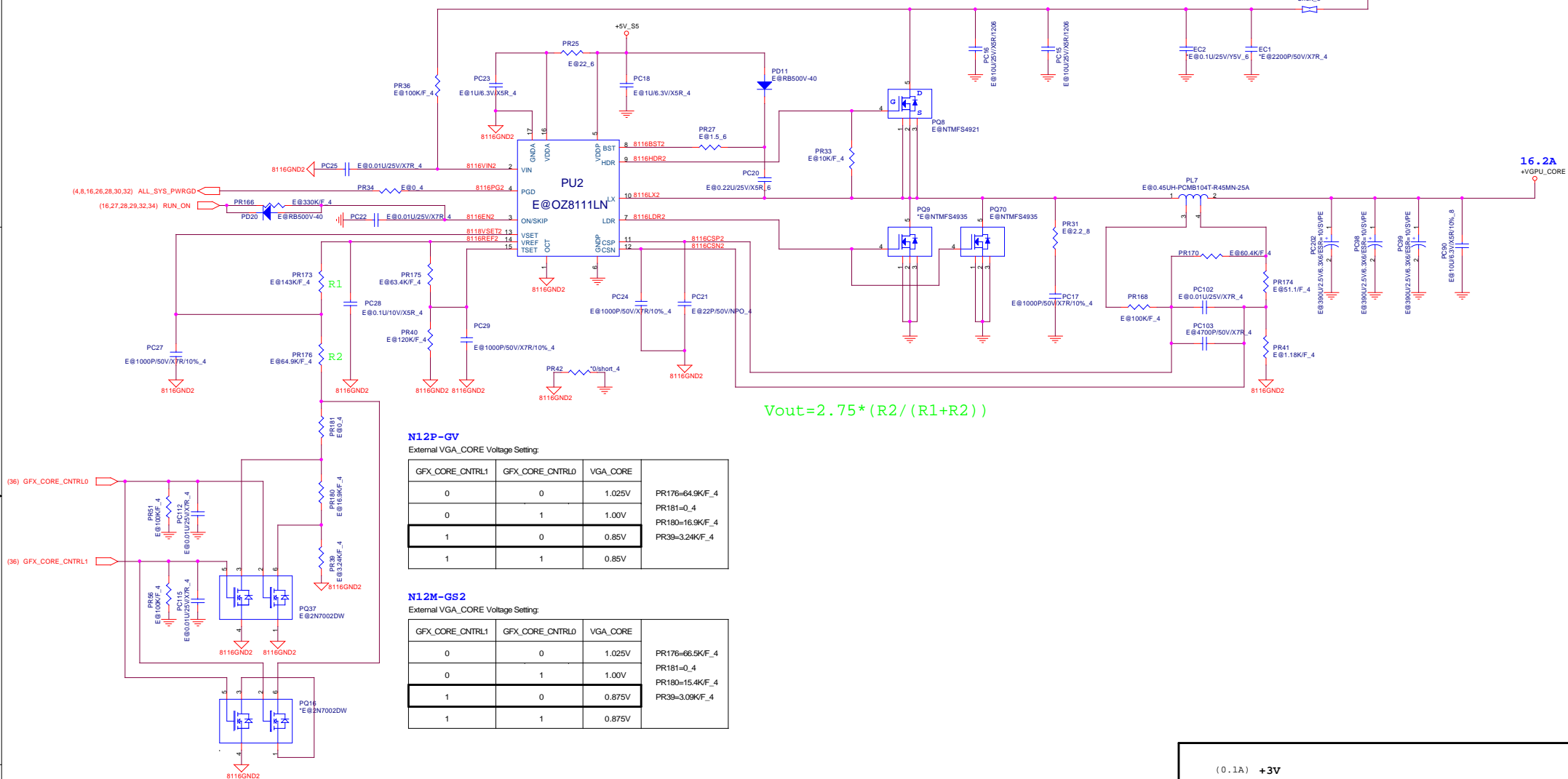
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



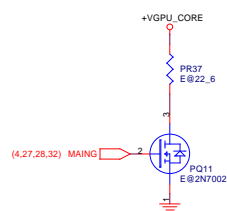
H_SNB_IVB#_PWRCTRL	+1.05V_VTT
0	1.0V
1	1.05V



VID 0	VCCSA_SEL	+0.85V
0	0	0.9V
0	1	0.8V
1	0	0.75V
1	1	0.65V



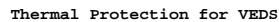
## Dis-charge



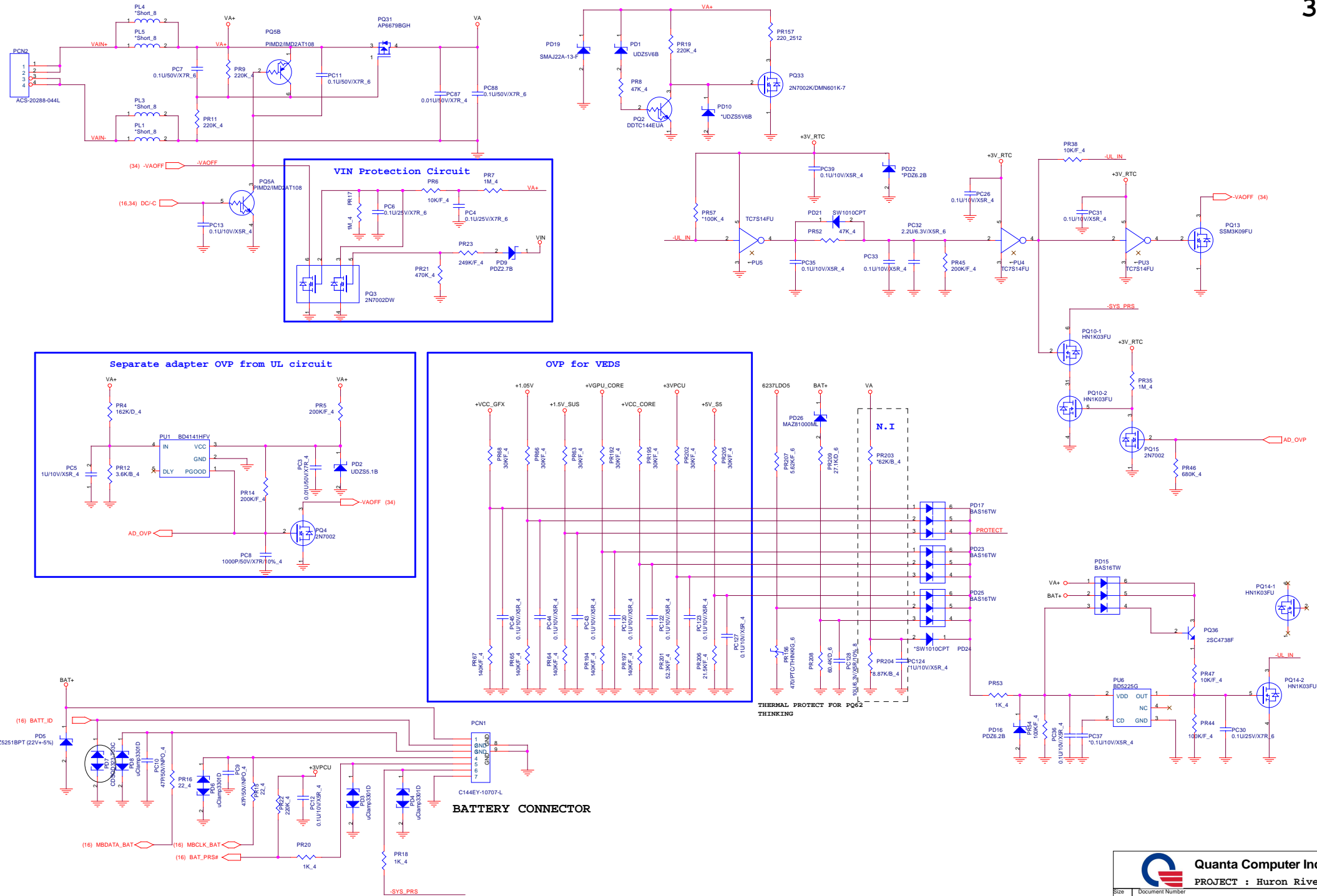
UMA GFX DISABLE



(0.1A) +3V  
(2A) +1.05V  
(6A) +1.5V







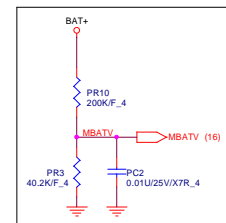
Quanta Computer Inc.  
PROJECT : Huron River

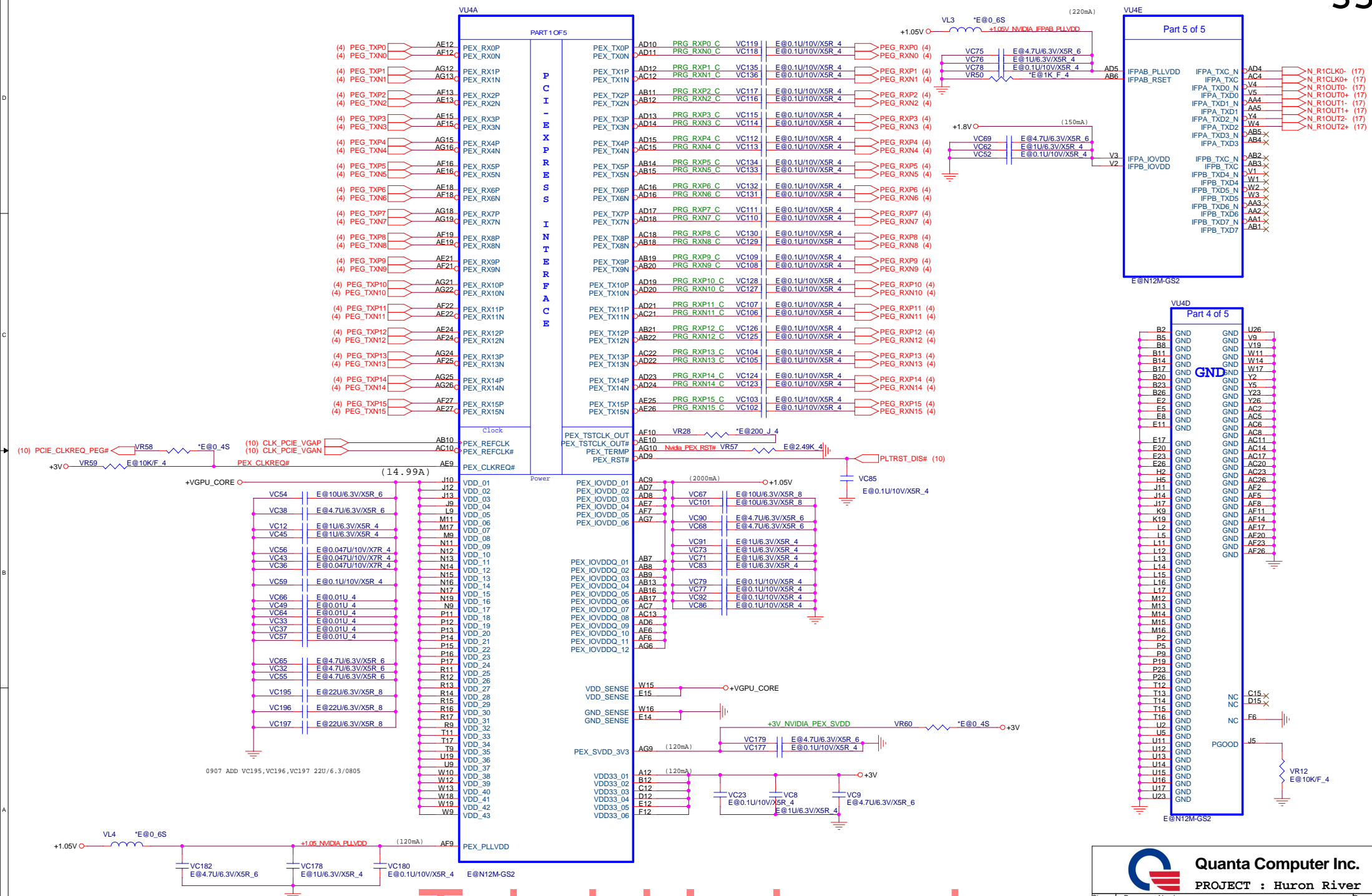
Size Document Number  
BAT INADA INUL  
Rev 1A

1. Level 1 Environment-related Substances Should Never be Used.

2. Recycled Paper and Coated Wire should be procured from Green Partners.

Date: Sunday, April 03, 2011 Sheet 33 of 39





### External VGA CORE Voltage Settings:

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=64.9K/F_4
0	1	1.00V	PR181=0_4
1	0	0.85V	PR180=16.9K/F_4
1	1	0.85V	PR39=3.24K/F_4

N12M-GS2

### External VGA CORE Voltage Setting:

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	VGA_CORE	
0	0	1.025V	PR176=66.5K/F_4
0	1	1.00V	PR181=0_4
1	0	0.875V	PR180=15.4K/F_4
1	1	0.875V	PR39=3.09K/F_4

## Logical Strap Bit Mapping

Resistor Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

### N12M Strap Bit Define

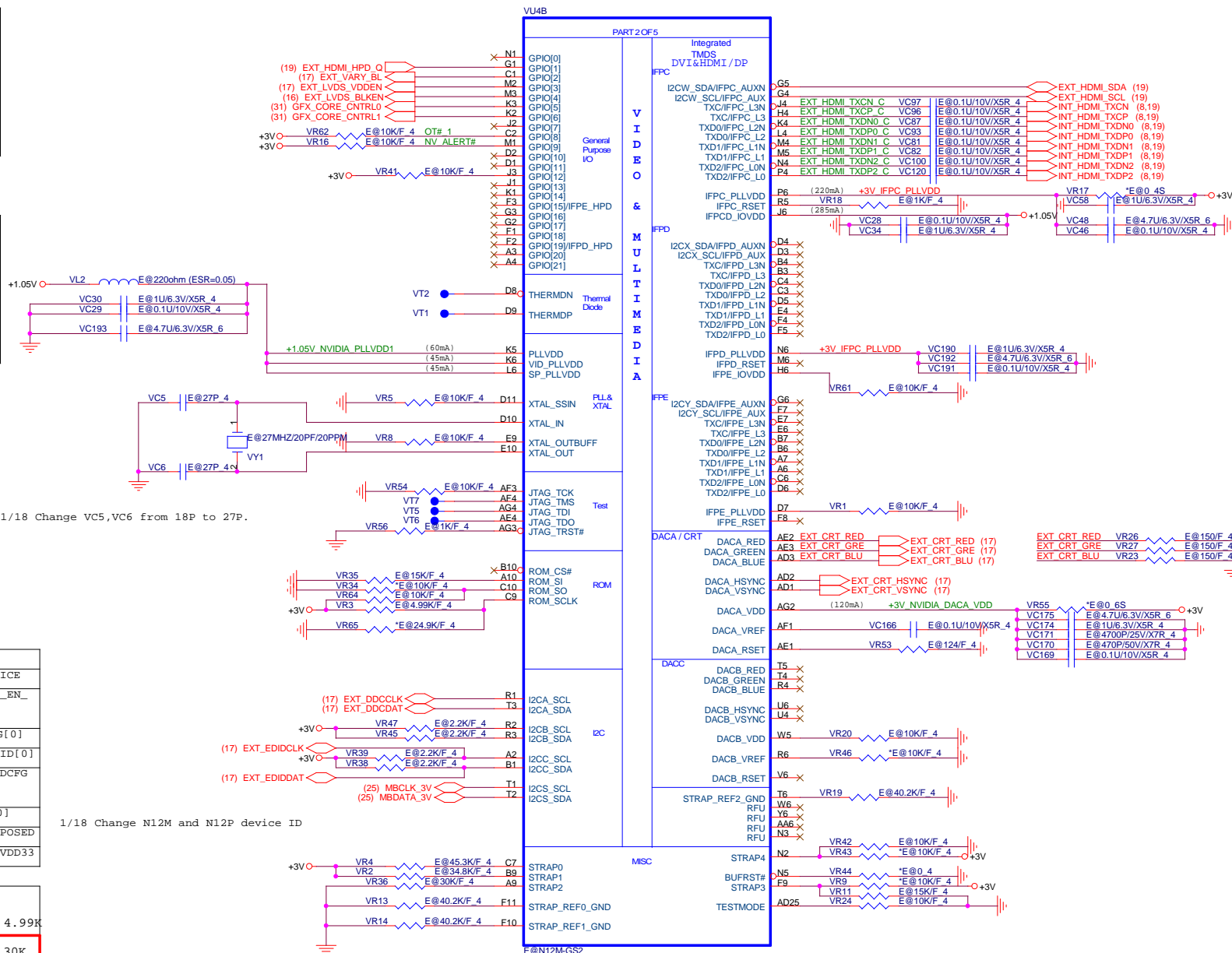
Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	FB[1]	FB[1]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33

```
for device ID
```

For N12P VR3 pull high 4.99K VR65 NC VR36 Pull down 4.99K

For N12M VR3 pull high 4.99K VR65 NC VR36 Pull down 30K

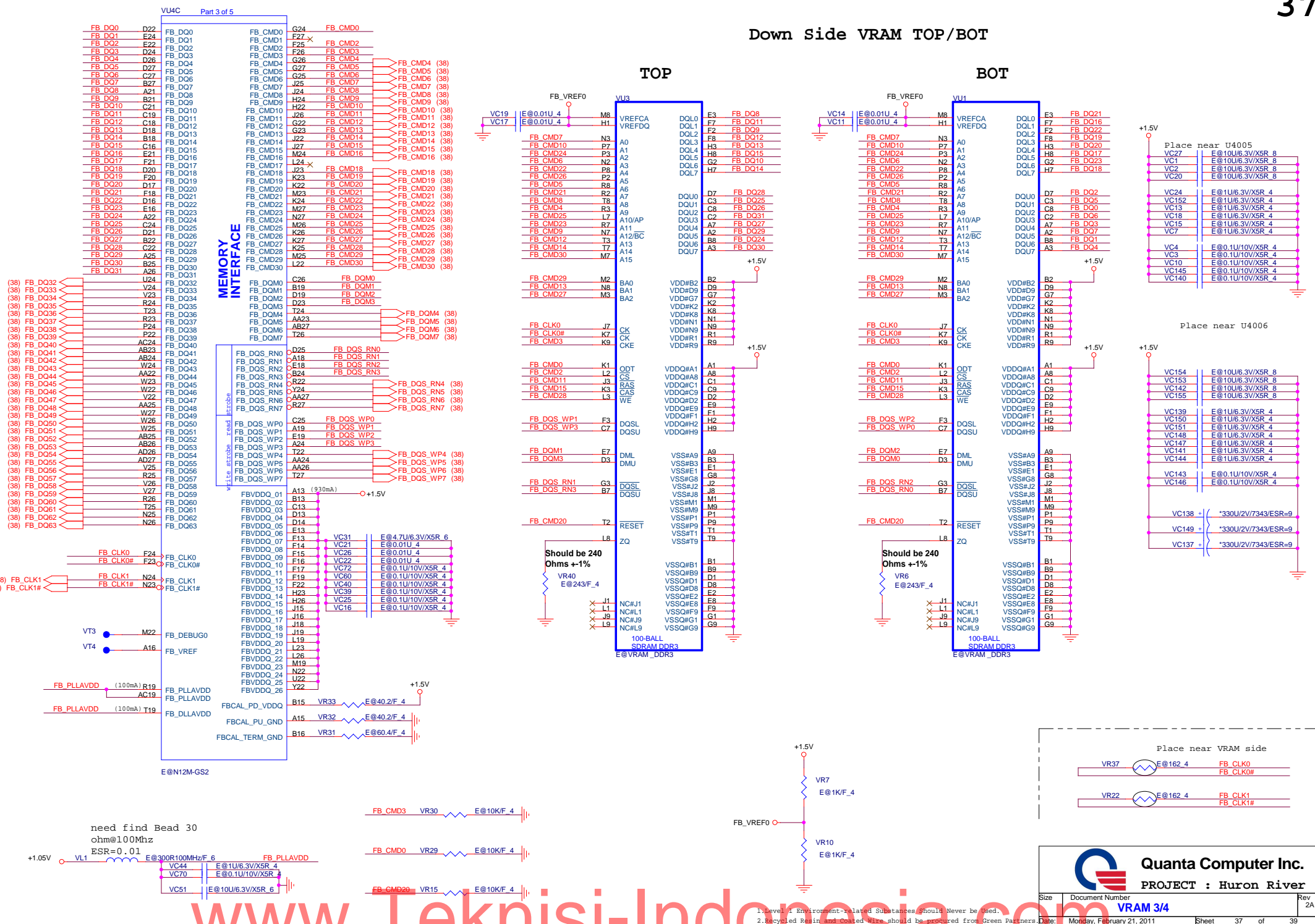
	VRAM Capacity	VRAM Vender	ID	VR35	P/N	P/N
N12M	64Mx16 DDR3	Hynix	0010	PD15K	H5TQ1G63DFFR-12C	
		Samsung	0011	PD20K	K4WL1G1646G-BC12	
	128Mx16 DDR3	Hynix	0110	PD35K	H5TQ <del>GG63BFR</del> -12C	
		Samsung	0111	PD45K	K4W2G1646C-HC12	



## Down Side VRAM TOP/BOT

TOP

BOT

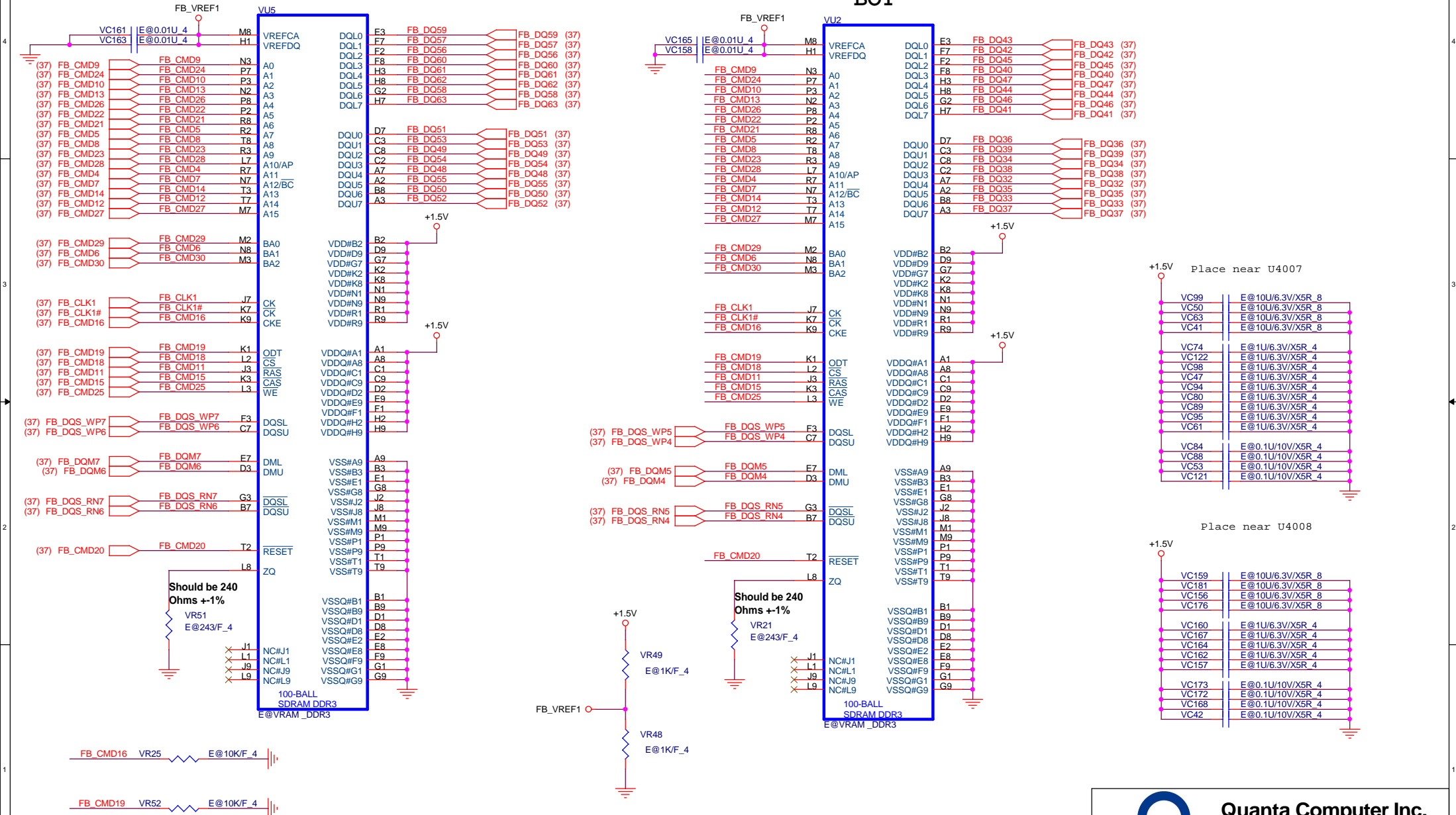




## Up Side VRAM TOP/BOT

**TOP**

**BOT**





## USB PORT Architecture for EVT

PORT 0	IO Port
PORT 1	IO Port
PORT 2	IO Port
PORT 3	N/A
PORT 4	IO Port
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	Camera
PORT 10	N/A
PORT 11	N/A
PORT 12	WiMax
PORT 13	BlueTooth

## PCIE BUS

PORT 1	WLAN Port
PORT 2	N/A
PORT 3	N/A
PORT 4	CARD READER
PORT 5	N/A
PORT 6	GLAN(RTL8111E)
PORT 7	N/A
PORT 8	N/A

## SM BUS MBCLK/MBDATA

ISL88731CHRTZ	0001 001X
NVIDIA	1001 111X

## SATA BUS

PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	ODD
PORT 4	N/A

Board ID0 (N12M/N12P)	N12M	N12P
R294	Stuff	No Stuff
R297	No Stuff	Stuff

Board ID1 (VRAM Vendor)	Samaung	Hynix
R47	Stuff	No Stuff
R48	No Stuff	Stuff

Board ID2 (VRAM 1G/512M)	1G	512M
R39	Stuff	No Stuff
R27	No Stuff	Stuff

	DGPU_PRSENT#(GPIO39)	BOARD_ID0 (GPIO16)	BOARD_ID1 (GPIO6)	BOARD_ID2 (GPIO17)
UMA	0	0	0	0
N12M-GS2_SAM_512MB	1	1	1	0
N12M-GS2-SAM_1GB	1	1	1	1
N12M-GS2-HYN_512MB	1	1	0	0
N12M-GS2-HYN_1GB	1	1	0	1
N12P-GV_SAM_512MB	1	0	1	0
N12P-GV-SAM_1GB	1	0	1	1
N12P-GV-HYN_512MB	1	0	0	0
N12P-GV-HYN1_1GB	1	0	0	1